ISEE IGEPv2 BOARD

IGEPv2 BOARD
Hardware Reference Manual
(Revision 1.21 26/10/2010)

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Integration Software and Electronics Engineering

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VERSION CONTROL

VERSION	DATE	ORIGIN	DESCRIPTION
1.00	19/03/2009	R&D	Initial version
1.02	20/05/2009	R&D	Board Configuration update.
1.10	24/07/2009	R&D	Update Hw Revision RB
1.11	21/09/2009	R&D	Document Update
1.12	24/09/2009	R&D	Document Update
1.13	23/10/2009	R&D	Document Update
1.14	18/11/2009	R&D	Document Update
1.15	9/03/2010	R&D	Update Hw Revision RC
1.16	15/05/2010	R&D	Document Update
1.17	6/07/2010	R&D	Document Update
1.18	9/07/2010	R&D	Document Update
1.19	31/08/10	R&D	Document Update
1.20	1/10/10	R&D	Document Update
1.21	26/10/10	R&D	Document Update

1 COPYRIGHT NOTICE

2 WARRANTY

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund.

THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies ISEE 2007 SL from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

ISEE 2007 SL currently deals with a variety of customers for products, and therefore our arrangement with the user is not exclusive. ISEE assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.

Please read specifically, the Warnings and Restrictions notice in this manual prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on IGEPV2 environmental and/or safety programs, please contact with ISEE (support@iseebcn.com).

No license is granted under any patent right or other intellectual property right of ISEE covering or relating to any machine, process, or combination in which such ISEE products or services might be or are used.

WARRANTY: IGEPV2 is warranted against defects in materials and workmanship for a period of 1 year from purchase. This warranty does not cover any problems occurring as a result of improper use, modifications, exposure to water, excessive voltages, abuse, or accidents. All boards will be returned via standard mail if an issue is found. If no issue is found or express return is needed, the customer will pay all shipping costs.

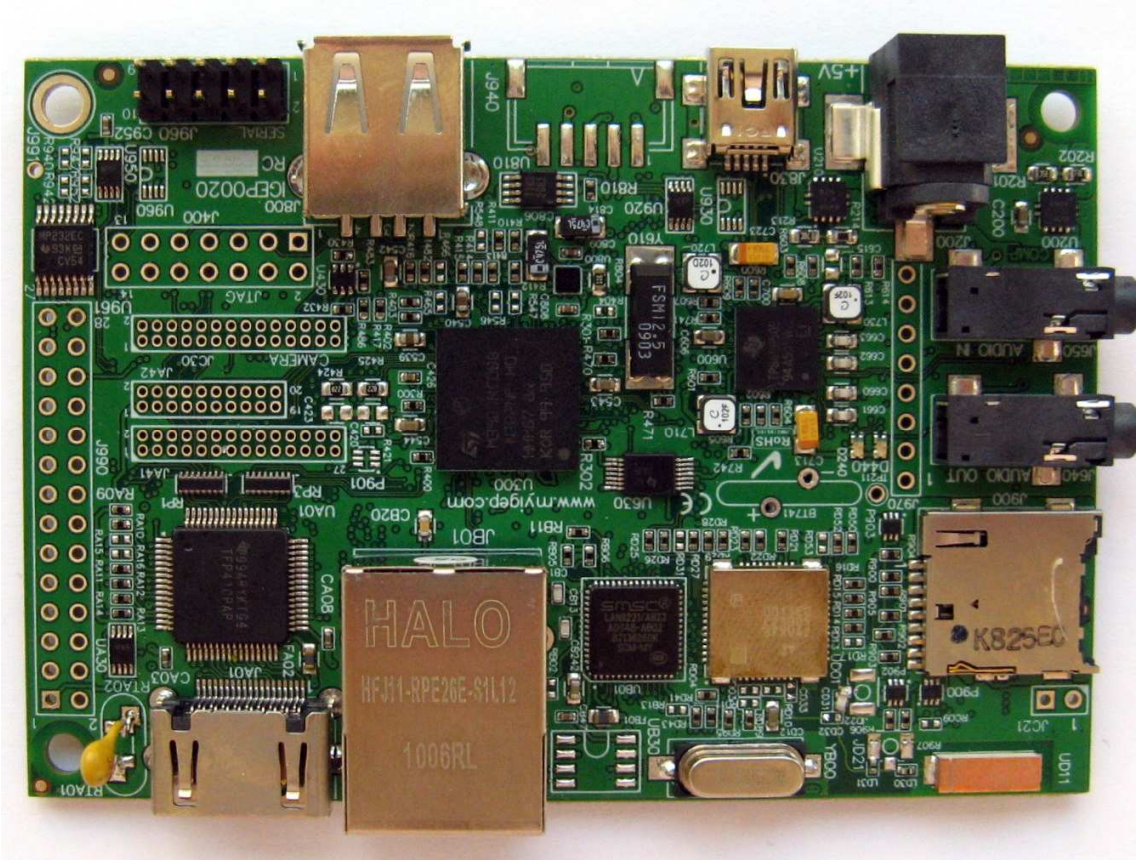
ISEE IGEP platform web site: http://www.igep.es

ISEE IGEP wiki: http://labs.igep.es

ISEE shop: http://shop.igep.es or https://shop.igep.es

ISEE Software Repositories: http://git.igep.es

3 ISEE IGEPV2 BOARD FEATURES



Description	Characteristics
Processor	OMAP3530 (ARM Cortex-A8)
Processor Speed	720 Mhz
Memory SDRAM	512 MBytes LPDDR SDRAM – 200 Mhz
Nand Flash	512 Mbytes
DSP	TMS320DM64+
DSP Speed	430 Mhz
Video 3D Accelerator	PowerVR SGX 530
Power Management	TPS65950
Debug	Console RS232 + JTAG Interface
PCB size	93 x 65 x 1.6 mm

Indicators	2 Bicolor USER LEDS
USB 2.0 LS/FS/HS OTG	1 Mini AB USB socket connector (dual slave and host role)
USB 2.0 HS HOST	1 Type A USB socket connector (standard USB host)
Audio stereo in/out	3.5mm standard stereo audio jack
microSD	microSD connector (SD and SDHC cards supported)
DVI video output	DVI-D using HDMI connector. (video and TS lines are available in expansion connector also).
Power	5Vcc / 1A 3.5mm socket connector for wall plug or JST Connector
Expansion connector	Power 5V and 1.8V, UART, McBSP, McSPI, I2C, GPIO, RS485 with transceiver, Keyboard.
Wifi	IEEE 802.11b/g 2,4GHz
Bluetooth	2.0
Antenna WiFi/Bluetooth	1 shared internal antenna (integrated on PCB)
Ethernet	10/100 MB BaseT (RJ45 connector with led link/activity)
Temperature Range	Commercial (0 to 70 Cº) and Industrial range (-40 to +80 Cº Degrees) are available (**Contact ISEE sales**)

WARNING: IGEPv2 BOARD CAN ONLY BE POWERED WITH 5V DC

POWER SUPPLY OR THE BOARD WILL BE DAMAGED!

The following sections provide more detail on each feature and components on the IGEPv2 BOARD.

3.1 ISEE IGEPV2 BOARD GENERAL SPECIFICATIONS

OMAP Processor

The IGEPv2 BOARD uses the OMAP3530 version ES3.1 and comes in a 0.4mm pitch memory POP package on it.

POP (Package on Package) is a technique where the memory, NAND and SDRAM, are mounted on top of the OMAP3530. For this reason, when looking at the IGEPv2 BOARD, you will not find an actual part labeled OMAP3530.

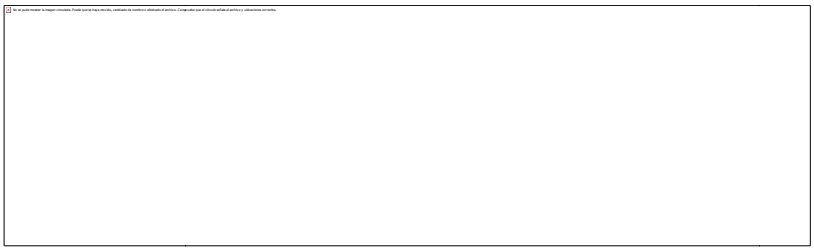


Figure 1 POP Package

Memory

The memory is mounted on top of the processor as mentioned. The key function of the POP memory is to provide:

- 4Gb NAND x 16 (512MB)
- 4Gb LP-DDR SDRAM x32 (512MB @ 200MHz)

Power Management

The TPS65950 is used on the board to provide power to the IGEPv2 Board with the exception of the 3.3V regulator which is used to provide power to the DVI-D encoder and RS232 driver. In addition to the power it also provides:

- Stereo Audio Out
- Stereo Audio in
- Power on reset
- USB OTG PHY
- Status LED

USB 2.0 LS/FS/HS OTG

On the board a single USB 2.0 OTG Port is provided.

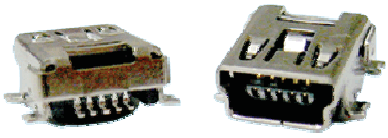


Figure 2 USB OTG connector

It is not possible to power the board with the OTG connector.

USB 2.0 HS HOST

On the board a single USB 2.0 HS HOST port is provided via a USB Type A socket connector. Hardware provides power on/off switch control and up to 500mA of current limit at 5V.

Figure 3 USB HOST connector

USB HOST Port supports only high speed devices (USB 2.0 HS devices). In order to support low speed devices (USB 1.0 LS devices) or full speed devices (USB 1.1 FS devices), external USB 2.0 HUB must be used.

WIFI

IEEE802.11b/g compliant.

Chipset based on Marvell 88W8686. The 88W8686 integrates a RF transceiver operating at 2.4GHz, a physical layer, a media access controller, and an ARM processor into a single die.

BLUETOOTH

Bluetooth 2.0 compliant.

Class 2, 2.5 mW (4 dBm) ~10 meters

Version 2.0 + EDR 3 Mbit/s

ETHERNET

A RJ45 connector is provided for the Ethernet Auto-MDIX Full Duplex 10/100 Base T interface.

There is a EEPROM (U830) memory for MAC configuration (Not populated).

NOTE: Contact ISEE sales for custom assembly boards.

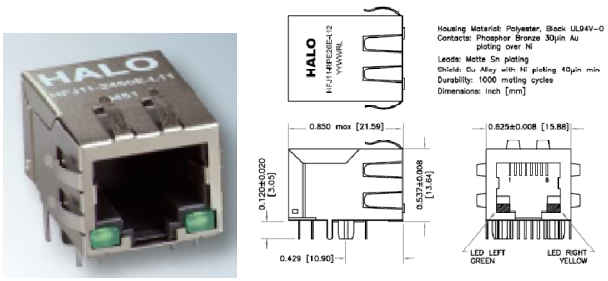


Figure 4 ETHERNET connector

This connectors come with link and activity status led.

Stereo Audio Output Connector

A 3.5mm standard stereo output audio jack is provided to access the stereo output of the onboard audio CODEC. The Audio CODEC is provided by the TPS65950.

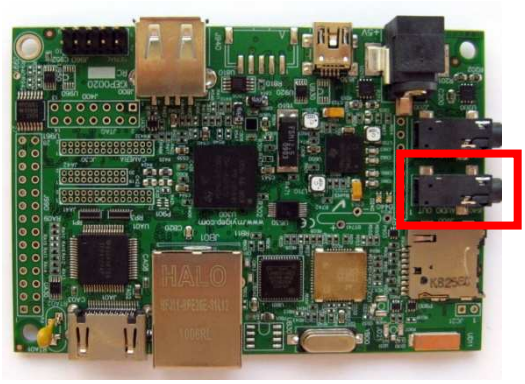


Figure 5 Stereo Output connector location

Stereo Audio In connector

A 3.5mm standard stereo audio input jack is provided to access the stereo input of the onboard audio CODEC.

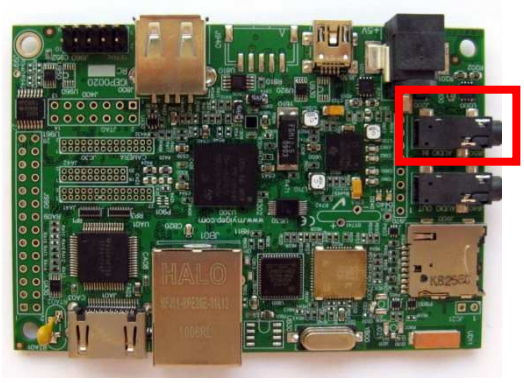


Figure 6 Stereo Input connector location

DVI-D Connector

The IGEPv2 BOARD can drive a LCD panel equipped with a DVI-D digital input. This is the standard LCD panel interface of the OMAP3530.

Figure 7 HDMI connector

DDC2B (Display Data Channel) or EDID (Enhanced Display ID) support over I2C is provided in order to allow the identification of the LCD monitor type and settings.

The IGEPv2 BOARD does not support the full HDMI interface and is used to provide the DVI-D interface portion only. The user must use a HDMI to DVI-D cable or adapter to connect to a LCD monitor. A standard HDMI cable can be used when connecting to a monitor with and HDMI connector.

LCD and touchscreen header

A pair of 1.27mm pitch 2x10 headers are provided to have access to the LCD signals and touchscreen control (IGEPv2 Revision B boards). On IGEPv2 Revision C boards, JA41 connector is wider and enhanced with additional LCD bits depth. All IGEPv2 boards (Revisions B and C) are mechanical, electrical and logical compatible.

This allows for the creation of LCD boards to support different LCD panels.

microSD Connector

A microSD connector is provided for microSD cards form factor.

The microSD memory card is the smallest memory card available commercially, with the lowest price per capacity and the highest capacity. At 15 mm × 11 mm × 1 mm (about the size of a fingernail), it is about a quarter the size of an SD card.

The microSD connector supports SD and SDHC cards. SDHC (Secure Digital High Capacity, SD 2.0) is an extension of the SD standard which increases card's storage

capacity up to 32GB. SDHC cards shares the same physical and electrical form factor as older (SD 1.x) cards, allowing SDHC-devices to support both newer SDHC cards and older SD-cards.

RS232

IGEPv2 Revision B boards provide only UART3 with RS232 levels on J960.

IGEPv2 Revision C boards provide both UART1 and UART3 with RS232 levels on J960. [*Contact ISEE sales for custom assembly boards for UART2 port*]

RS485

The IGEPv2 board comes with 1 x RS485 on JST connector J940 (UART1). On IGEPv2 Revision B are default populated. On IGEPv2 Revision C, RS485 are not default populated. [***Contact ISEE sales*** *for custom assembly boards for RS485 feature*].

ANALOG TO DIGITAL CONVERTER (A/D)

The IGEPv2 BOARD could come with one ADC (Analog to digital converter) device. The analog signal inputs from U.FL HIROSE connector (located at the bottom) or two 2,54mm pins header.

Several ADC devices can be populated. For example:

- ADC-SPI 3MSps 3V3 (LTC2366)
- ADC-SPI 1MSps 5VDC (ADC121S101)

Indicators

There are two bicolor LEDs on the Board that can be controlled by the user. In total are like 4 individual leds and 16 color schemes

- Three leds are controlled via GPIO pins on the OMAP3530 Processor
- One is programmed via the I2C interface on the TPS65950

Power Connector

Power will be supplied via the DC power jack (or via JST connector J940).

JTAG Connector

A 14 pin JTAG header is provided on the board to facilitate the SW development and debugging of the board by using various JTAG emulators. The interface is at 1.8V on all signals. Only 1.8V CMOS levels are supported. **DO NOT expose the JTAG header to 3.3V.**

Expansion Header

An option for a single 28 pin header is provided on the board to allow the connection of various expansion cards that could be developed by the users or other sources. Due to multiplexing, different signals can be provided on each pin providing more that 24 actual signal accesses.

3.2 SYSTEM BLOCK DIAGRAM

3.2.1 IGEPV2 REVISION B BOARD SERIES BLOCK DIAGRAM

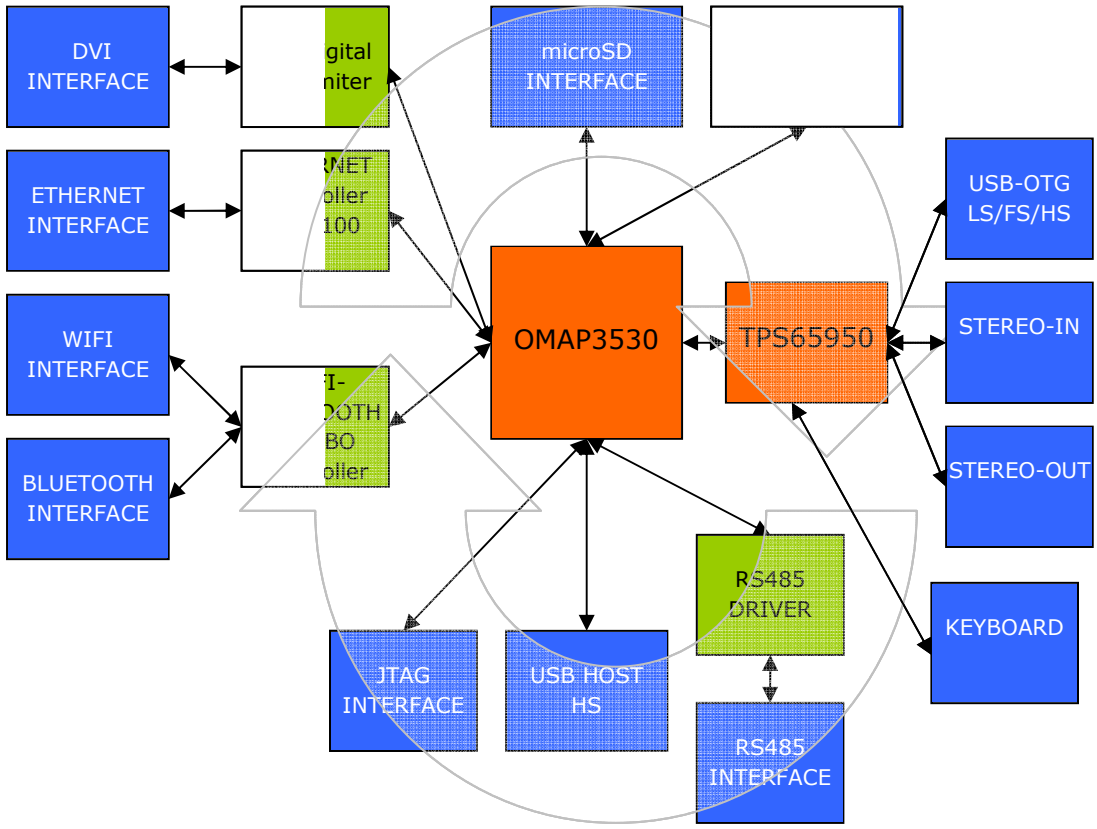


Figure 8 IGEPv2 Revision B board series block diagram

3.2.2 IGEPV2 REVISION C BOARD SERIES BLOCK DIAGRAM

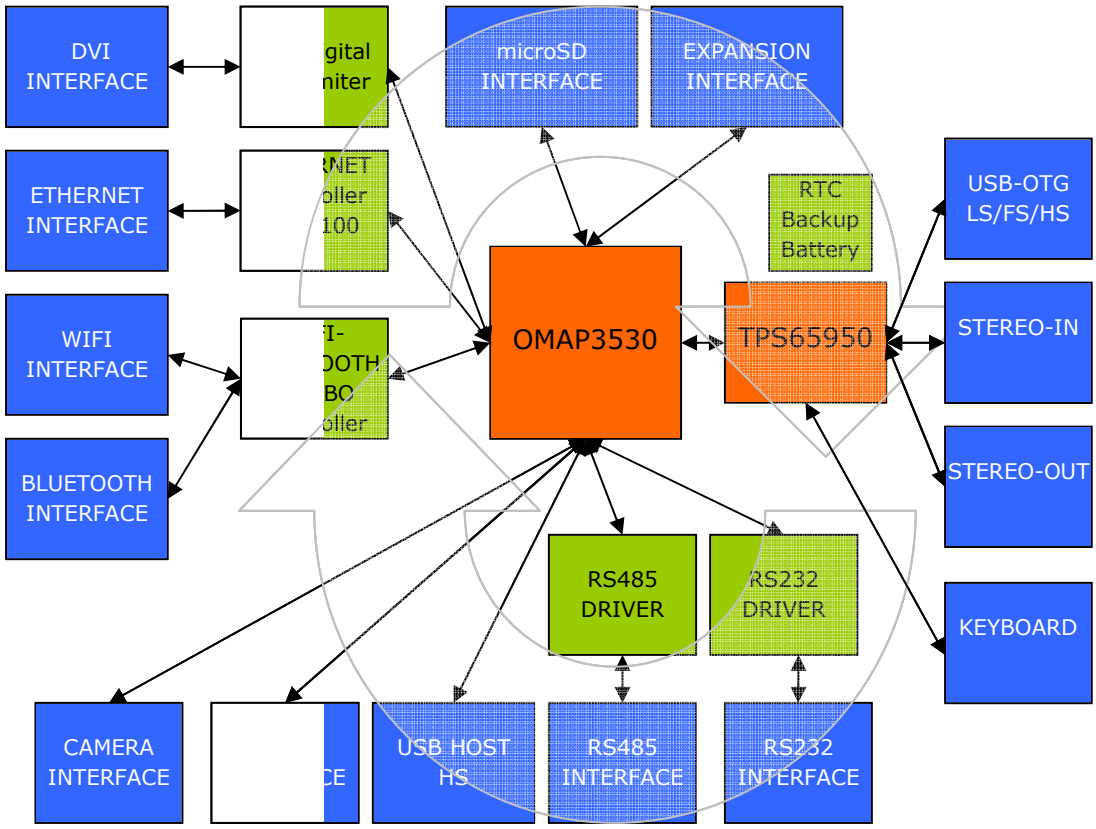


Figure 9 IGEPv2 Revision C board series block diagram

3.2.3 IGEPV2 REVISION C BOARD SERIES IMPROVEMENTS

Main goals of new IGEPv2 revision C series are:

- RTC Battery Backup for TPS65950 (Super Capacitor or Rechargeable Battery)
- Updated TFT interface from 18bit to 24bit.
- New Camera Connector (full OMAP interface on a new 28pin header connector)
- Optional high speed 3MBps ADC (Hirose U.FL connector or two pin header)
- Added second RS232 UART on J960 (Now 2 UARTs on J960, UART3+UART1)
- Changed JD22 from GSC Murata connector to Hirose U.FL connector
- Added optional second external antenna (Hirose U.FL connector)
- New GPIO to physically reset BT module
- Added resistors for hardware UART selection
- Non-populated parts:
    - J400 JTAG connector
    - J990: GPIO expansion connector
    - J970: 4x4 keyboard connector
    - JD22: External wifi antenna connector
    - JA41 and JA42: TFT interface
    - JC30: Camera interface
    - UC20 3MBps ADC + JC21 Hirose connector

Contact ISEE sales for custom assembly boards for fully previous IGEPv2 revision B compatible (mechanical, electrical and logical) on IGEP0020-RCx PCBs.

3.3 GENERAL VIEW

3.3.1 IGEPV2 REVISION B BOARD SERIES VIEW

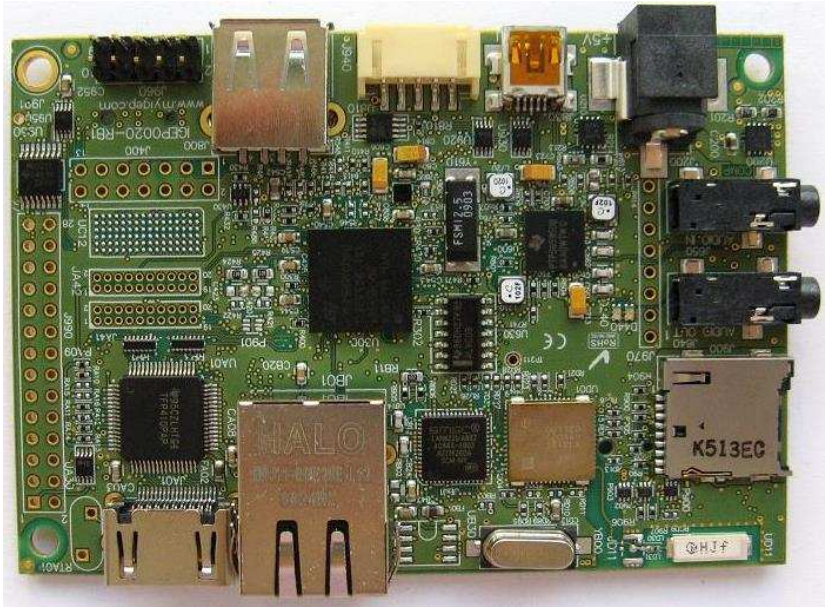


Figure 10 IGEPv2 revision B board top side components

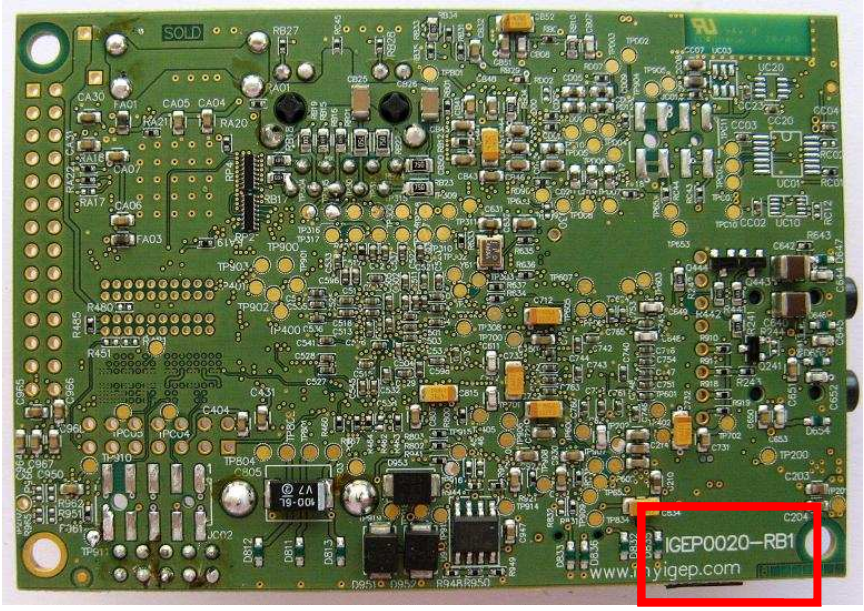


Figure 11 IGEPv2 revision B board bottom side components

3.3.2 IGEPV2 REVISION C BOARD SERIES VIEW

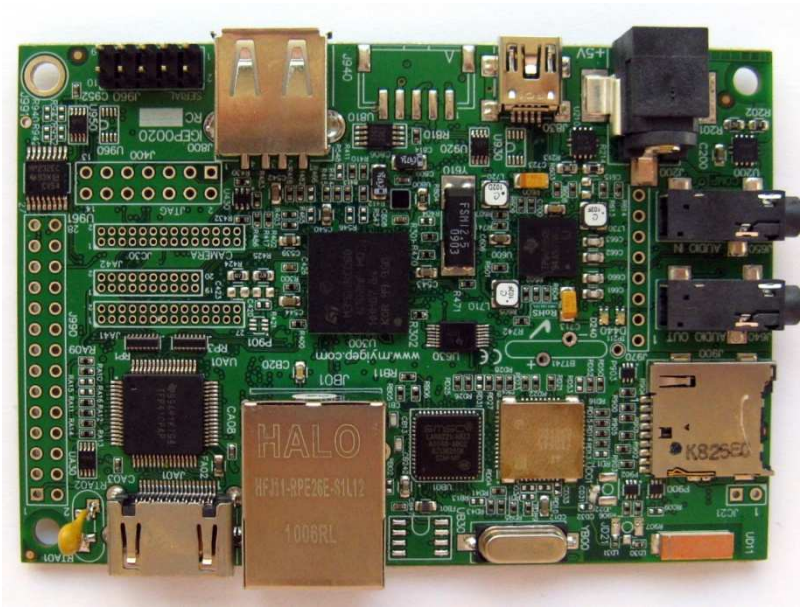


Figure 12 IGEPv2 revision C board top side components

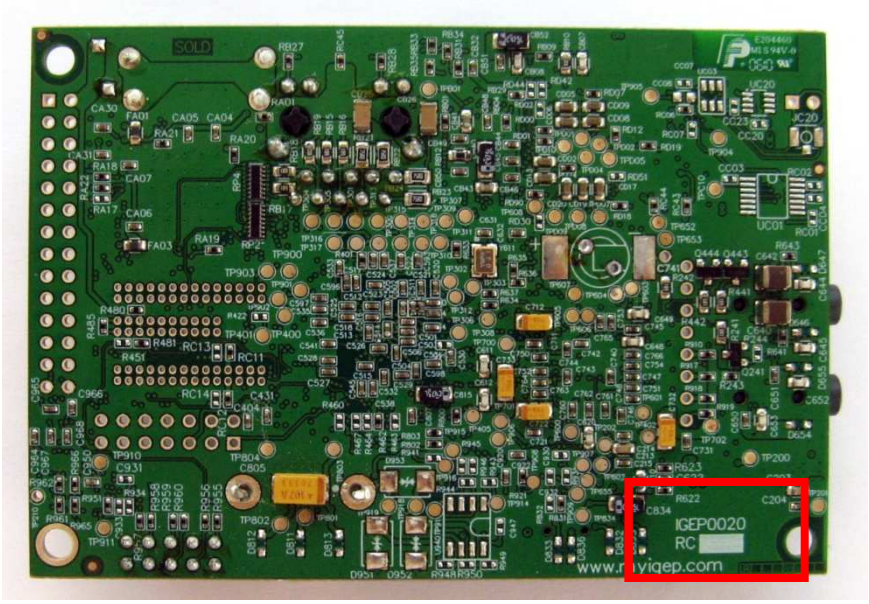


Figure 13 IGEPv2 revision C board bottom side components

3.4 MECHANICAL SPECIFICATION

3.4.1 IGEPV2 REVISION B BOARD SERIES MECHANICAL

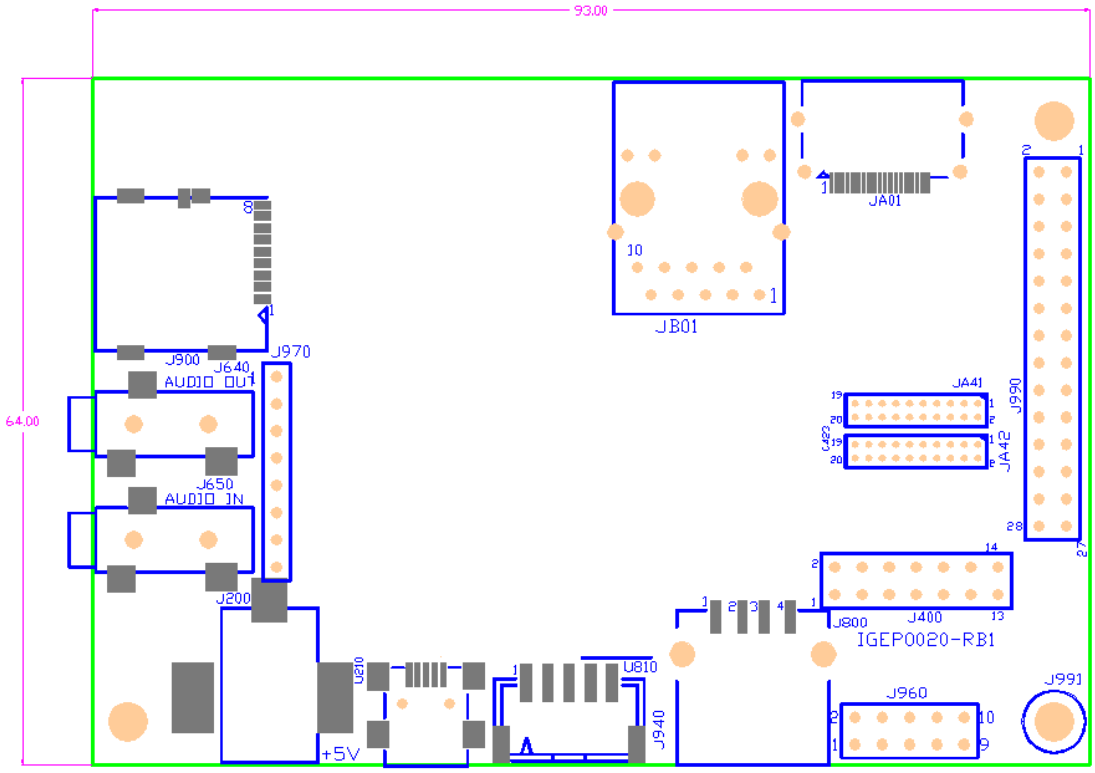


Figure 14 IGEPv2-RB Top view mechanical specification

Get Mechanical drawings on:

http://www.igep.es → User Menu → Download → 01-Products → IGEPv2 → HW_Mechanical

3.4.2 IGEPV2 REVISION C BOARD SERIES MECHANICAL

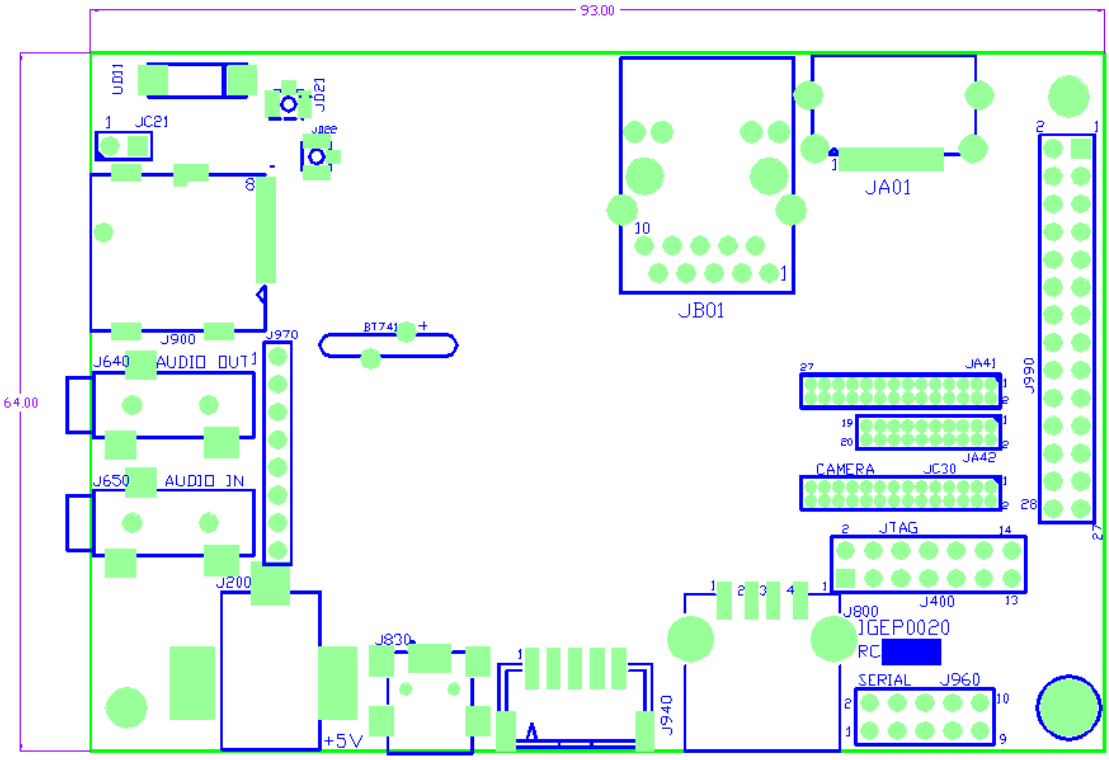


Figure 15 IGEPv2-RC Top view mechanical specification

Get Mechanical drawings on:

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3.5 ELECTRICAL SPECIFICATIONS

Specification	Min	Typ	Max	Unit
Power				
Input Voltage DC	4.8	5	5.2	V
Current DC		650	750	mA
USB 2.0 OTG				
High Speed Mode (HS)			480	Mb/s
Full Speed Mode (FS)			12.5	Mb/s
Low Speed Mode (LS)			1.5	Mb/s
USB 2.0 Host				
High Speed Mode (HS)			480	Mb/s
RS485				
Driver				
Input High Voltage	2			V
Input Low Voltage			0.8	V
Maximum Data Rate	250			Kbps
Receiver				
Output Voltage High	2.8			V
Output Voltage Low			0.4	V
Input Resistance	12	15		KOhms
JTAG				
Realview ICE Tool			30	MHz
XDS560			30	MHz
XDS510			30	MHz
Lauterbach(tm)			30	MHz
microSD				
Voltage Mode 1.8V	1.71	1.8	1.89	
Voltage Mode 3.3V	3.2	3.3		
Current			220	mA
Clock			48	MHz
DVI-D				
Pixel Clock Frequency	25		75	MHZ
High level output voltage		3.3		V
Swing output voltage	400		600	mVp-p
Maximum resolution	67.5	75	82.5	Ohms
Audio-In				
Peak-to-peak single-ended input voltage (0 dBFs)			1.5	Vpp
Total harmonic distortion (sine wave @ 1.02 kHz @ -1 dBFs)		-80	-75	dB
Total harmonic distortion (sine wave @ 1.02 kHz) 20 Hz to 20 kHz, A-weighted audio, Gain = 0 dB		-85	-78	dB
Audio-Out				
Load Impedance @100 pF	14	16		Ohms
Maximum Output Power (At 0.53 Vrms differential output voltage and load impedance = 16 Ohms)		17.56		mW
Peak-to-Peak output voltage			1.5	Vpp
Total Harmonic Distortion @ 0 dBFs		-80	-75	dB
Idle channel noise (20Hz to 20KHz)		-90	-85	dB
Ethernet				

Fully compliant with IEEE 802.3/802.3u				
10BASE-T and 100BASE-TX support				
Power supply		3.3		V
Wifi IEEE802.11b				
Specification		IEEE802.11b		
Frequency 2400 - 2500MHz	2400		2500	MHz
Data rate		1, 2, 5.5, 11		Mbps
Power Levels	15.5	17.5	19.5	dBm
Minimum Input Level Sensitivity 11Mbps (FER < 8%)	-	-87	-81	dBm
Maximum Input Level	-10	-5	-	dBm
Wifi IEEE802.11g				
Specification		IEEE802.11g		
Frequency 2400 - 2500MHz	2400		2483.5	MHz
Data rate		6, 9, 12, 18, 24, 36, 48, 54		Mbps
Power Levels	13	14.8	17.0	dBm
Minimum Input Level Sensitivity 11Mbps (FER < 8%)	-	-71	-65	dBm
Maximum Input Level	-20	-15	-	dBm
Bluetooth 2.0				
Bluetooth specification		2.0		
Channel spacing		1		MHz
Output Power	-4	0	+4	dBm
Frequency range (Rx/Tx)	2400		2483.5	MHz
Sensitivity (BER≦0.1%)				
1) 2402MHz - -81 -73 dBm	-	-81	-73	dBm
2) 2441MHz	-	-81	-73	dBm
3) 2480MHz	-	-79.5	-73	dBm
C/I Performance (BER≦0.1%)				
1) co-channel ratio (-60dBm input)	-	7.6	11	dBm
2) 1MHz ratio (-60dBm input)	-	-2.5	0	dBm
3) 2MHz ratio (-60dBm input)	-	-42.6	-30	dBm

4 WIFI/BLUETOOTH INTERFACE

WLAN: Chipset based on Marvell 88W8686. The 88W8686 integrates a RF transceiver operating at 2.4GHz, a physical layer, a media access controller, and an ARM processor into a single die.

BLUETOOTH: Chipset based on CSR BC4ROM/21e.

4.1 BLOCK DIAGRAM

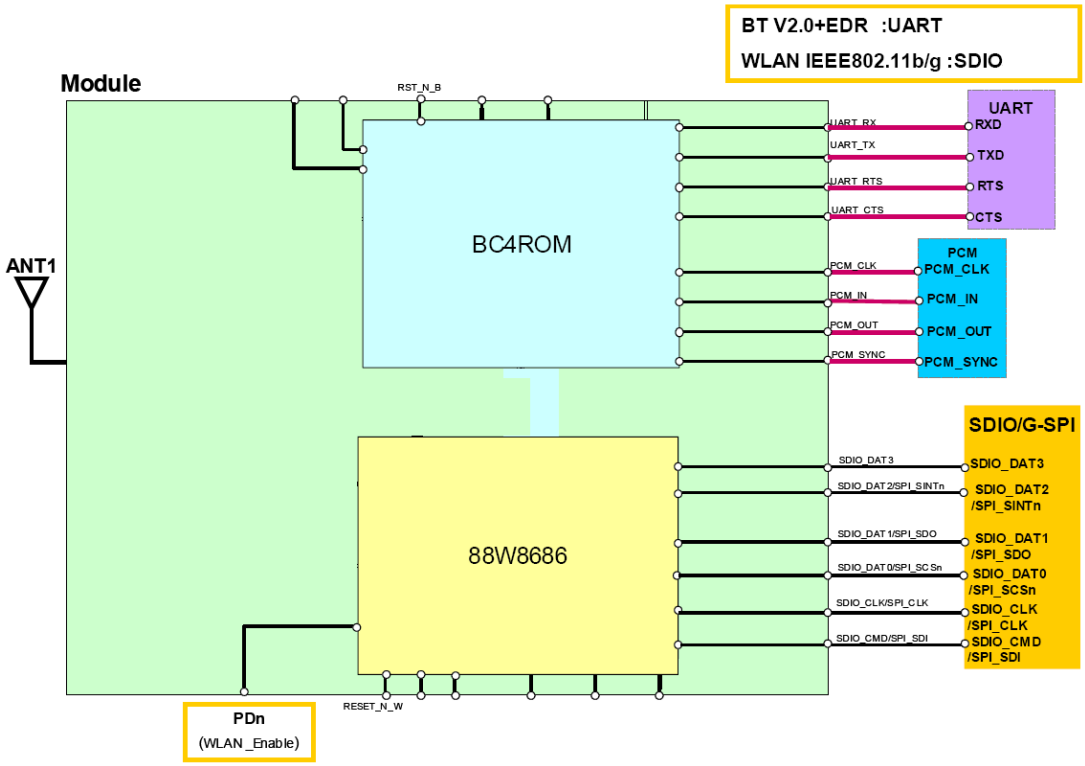


Figure 16 Wifi/Bluetooth Combo module block Diagram

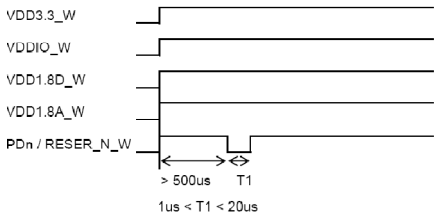
4.2 INTERFACES

Terminal Name	Type	System	Description
RST_N_B	I	BT	Reset (active low). It must be low for >5ms.
PCM_OUT	O	BT	Synchronous data output CMOS output, tri-statable with weak internal pull-down
PCM_SYNC	I/O	BT	Synchronous data sync, Bi Directional with weak internal pull-down.
PCM_IN	I	BT	Synchronous data input, CMOS input, with weak pull-down
PCM_CLK	I/O	BT	Synchronous data clock ,Bi Directional with weak internal pull-down.
UART_TX	O	BT	UART data output active high. CMOS output, tri-statable with weak internal pull-up.
UART_CTS	I	BT	UART clear to send active low. CMOS input with weak internal pull-down.

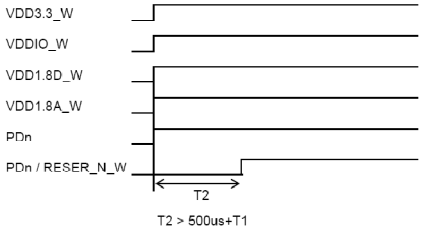
UART_RX	I	BT	UART data input active high. CMOS input, with weak internal pull up
UART_RTS	O	BT	UART request to send active low. CMOS input with weak internal pull-down.
SD_D3	I/O	WLAN	SDIO 4-bit Mode: SD_DAT[3] Data Line Bit [3] SDIO 1-bit Mode: SD_DAT[3] Reserved SDIO SPI Model: SD_DAT[3] Card Select (active low)
SD_D2 SPI_SINTn	I/O	WLAN	G-SPI Mode: SPI_SINTn G-SPI interrupt Output (active low) SDIO 4-bit Mode: SD_DAT[2] Data Line Bit [2] or Read Wait (optional) SDIO 1-bit Mode: SD_DAT[2] Read Wait (optional) SDIO SPI Model: SD_DAT[2] Reserved
SD_D1 SPI_SDO	I/O	WLAN	G-SPI Mode: SPI_SDO G-SPI Data Output SDIO 4-bit Mode: SD_DAT[1] Data Line Bit [1] SDIO 1-bit Mode: SD_DAT[1] Interrupt SDIO SPI Model: SD_DAT[1] Reserved
SD_D0 SPI_SCSn	I/O	WLAN	G-SPI Mode: SPI_SCSn G-SPI Chip Select input SDIO 4-bit Mode: SD_DAT[0] Data Line Bit [0] SDIO 1-bit Mode: SD_DAT[0] Data Line SDIO SPI Model: SD_DAT[0] Data Output
SD_CMD SPI_SDI	I/O	WLAN	G-SPI Mode: SPI_SDI G-SPI Data Input SDIO 4-bit Mode: SD_CMD Command/Response SDIO 1-bit Mode: SD_CMD Command Line SDIO SPI Model: SD_CMD Data Input
SD_CLK SPI_CLK	I/O	WLAN	G-SPI Mode: SPI_CLK G-SPI Clock Input SDIO 4-bit Mode: SD_CLK Clock Input SDIO 1-bit Mode: SD_CLK Clock Input SDIO SPI Model: SD_CLK Clock Input
RESET_N_W	I	WLAN	Internal pull-up. Reset (active low)
PDn	I	WLAN	Full Power Down (active low) 0 = full power down mode 1 = normal mode

4.3 POWER-ON RESET SEQUENCE FOR WLAN

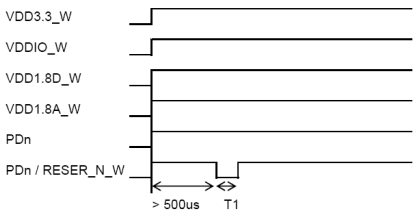
PDn / RESET_N_W tied together



PDn pin separated from RESET_N_W. Host can not pulse RESET_N_W pin.



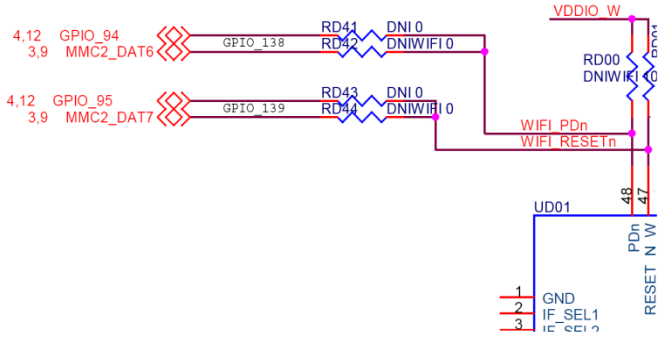
PDn pin separated from RESET_N_W. Host controls pulsing of RESET_N_W pin.



4.4 WLAN RESET/PDN PINS

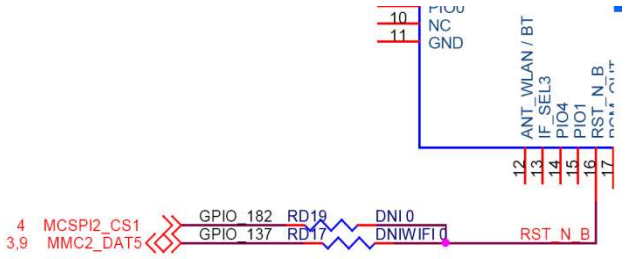
Reset can be done by using GPIO_94 or GPIO_138. By default RD41 is mounted.

Power down can be done by using GPIO_95 or GPIO_139. By default RD43 is mounted.



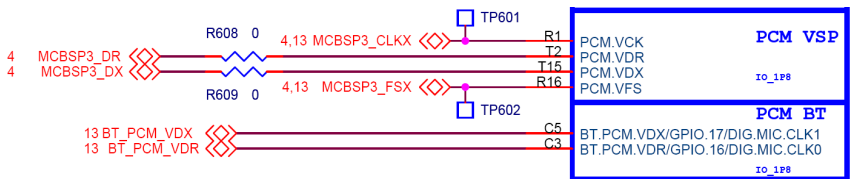
4.5 BLUETOOTH RESET PINS

Reset can be done by using GPIO182 or GPIO137. By default RD137 is mounted.



4.6 PCM INTERFACE

4.6.1 TPS65950 SIDE



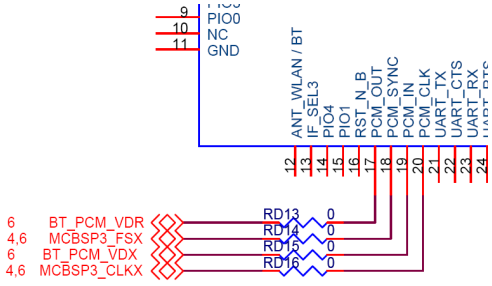
4.6.2 WIFI MODULE SIDE

PCM_OUT –Output- Synchronous data output CMOS output, tri-state with weak internal pull-down

PCM_SYNC -I/O- Synchronous data sync Bi Directional with weak internal pull-down.

PCM_IN – Input - Synchronous data input CMOS input, with weak pull-down

PCM_CLK - I/O - Synchronous data clock Bi Directional with weak internal pull-down.



5 CONNECTORS DESCRIPTION

This section will guide you through the ISEE IGEPv2 BOARD expansion connectors:

- Connector J200: main Power
- Connector J400: JTAG DEBUG
- Connector J940: Power + RS485
- Connector J960: UART3 Serial Debug. Only IGEPv2 Revision C, has also UART1 on J960.
- Connector J971: Keyboard Matrix 4x4
- Connector JA41-JA42: External TFT interface (18 bits). Only IGEPv2 Revision C, more TFT depth (24 bits)
- Connector J990: GPIO (muxed with UART2, MMC2, McBSP3, McSPI, I2C).
- Connector JD22: Optional external Wifi/bluetooth Antenna (IGEPv2 boards come with a default internal shared antenna).
- Connector JC30: Camera connector (Only IGEPv2 Revision C)
- Connector JC20: Optional A/D (Only IGEPv2 Revision C)
- Connector BT741: Optional RTC backup battery (Only IGEPv2 Revision C)

5.1 CONNECTOR J200: MAIN 5.0VCC POWER

The J200 connector is a power jack for main 5 VDC power.

It is a RASM722 switchcraft connector, Plug/Mating Plug Diameter 2.1mm ID, 5.5mm OD.

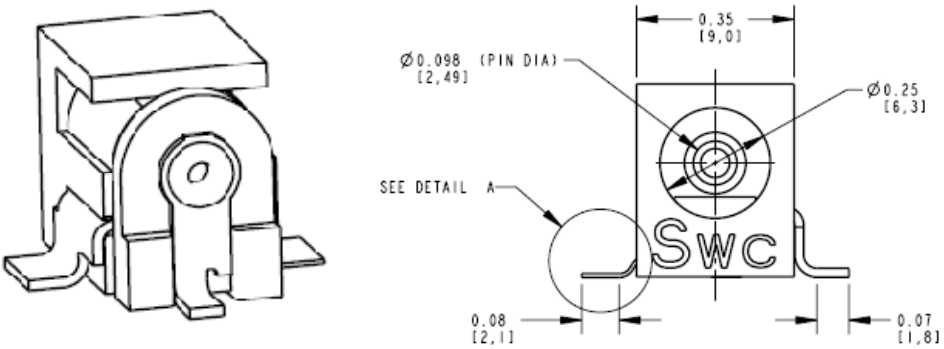


Figure 17 J200 detail

WARNING: IGEPv2 BOARD CAN ONLY BE POWERED WITH 5V DC POWER SUPPLY OR THE BOARD WILL BE DAMAGED!

5.2 CONNECTOR J400: JTAG DEBUG

The J400 connector is a 14 pins 2x7 dual row 2.54mm.

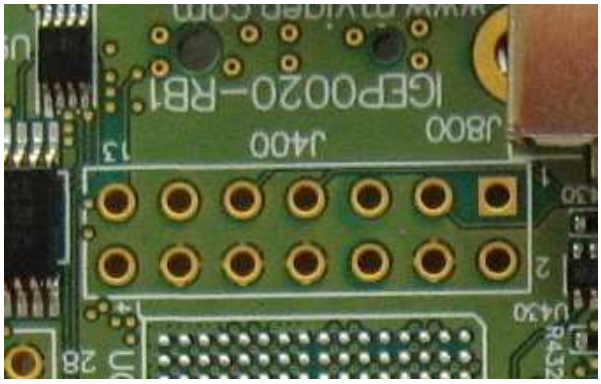


Figure 18 J400 detail

Pins 1, 2, 13 and 14 are labeled on the PCB. The connector is located as shows the figure below.

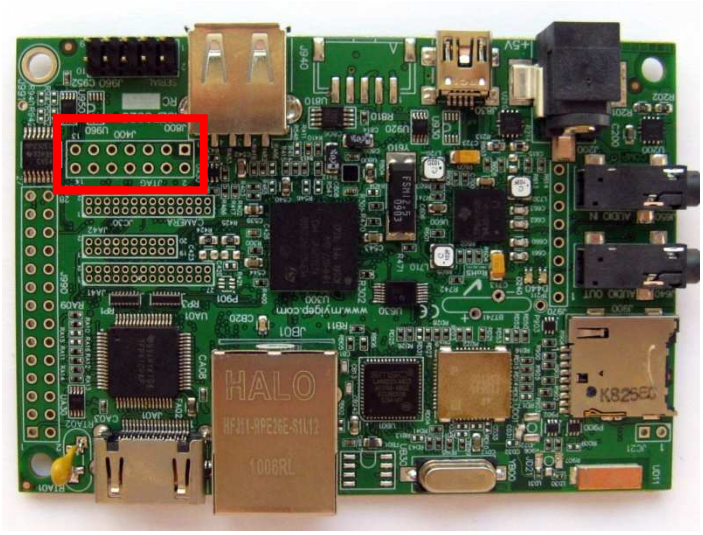


Figure 19 J400 location

The schematic below illustrate the pinout of the connector.

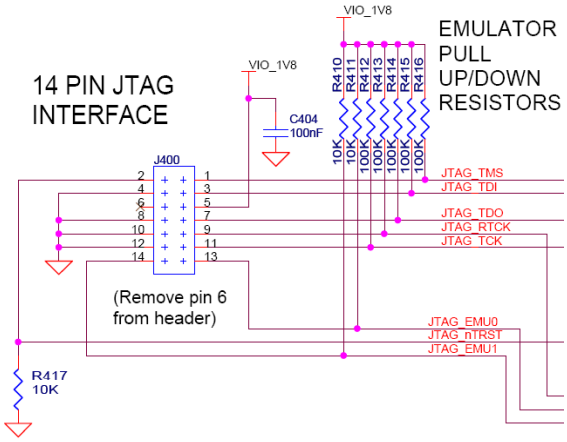


Figure 20 Schematic J400

WARNING: The JTAG signals go directly to OMAP processor. Improper use of this connector could result in damage of the processor.

Note: ISEE recommend JTAG Debugger XDS510+ USB from Spectrum Digital with Code Composer Studio

5.3 CONNECTOR J940: POWER + RS485

The J940 connector is a HEADER CONNECTOR PH SIDE 5POS 2MM SMD from JST (Part Number: S5B-PH-SM3-TB).

It matches to JST CONNECTOR HOUSING PH 5POS 2MM WHITE (Part Number: JST PHR-5) and JST TERMINALS CRIMP PH 24-30AWG (Part Number: JST SPH-002T-P0.5S). IGEPv2 don't include cable neither plug connector.

Pin 1 is labeled on the PCB. The connector is located as shown in the figure below.

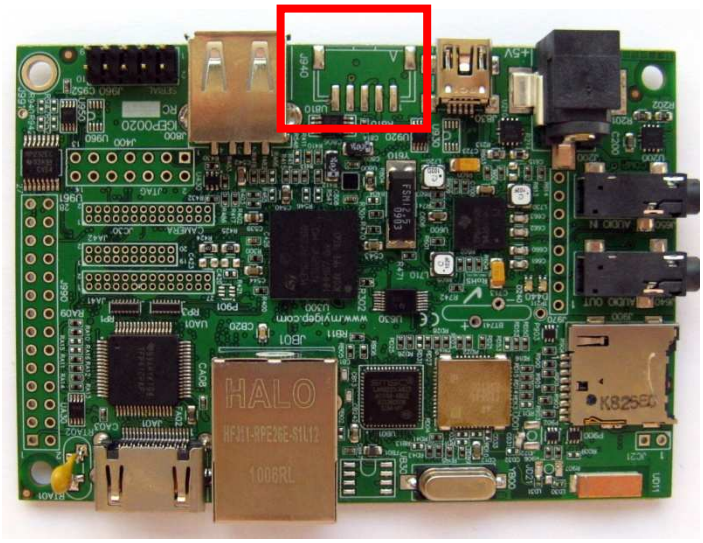


Figure 21 J940 location

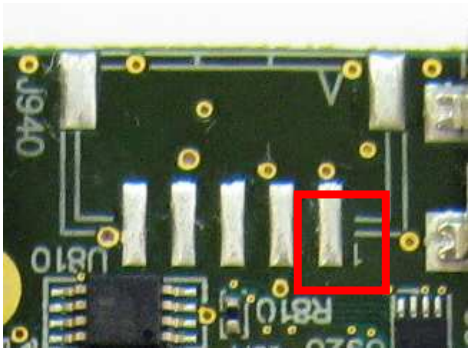


Figure 22 J940 detail pin 1

The schematic below illustrate the pinout of the connector.

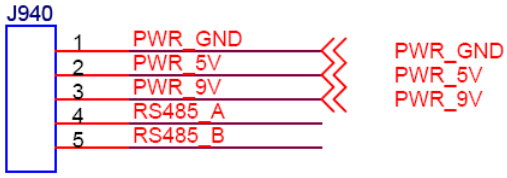


Figure 23 Schematic J940

User can use this connector to power the board with 5VDC. Use only 5V regulated DC.

The IGEPv2 BOARD does not use this 9v power supply. Only on IGEPv2 revision B, the PWR_9V input is directly routed to JC01 and J971 connectors. On IGEPv2 revision C is not available.

There is also a RS485 transceiver on the connector.

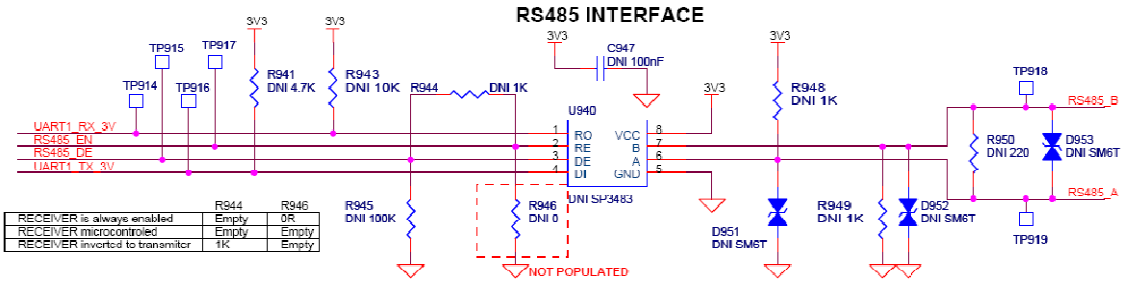


Figure 24 Schematic RS485 driver

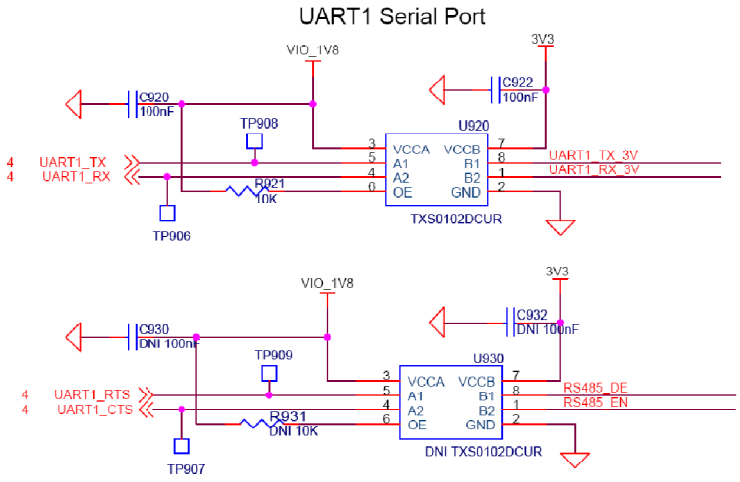


Figure 25 Schematic level-shifters for RS485 driver

5.4 CONNECTOR J960: SERIAL PORT DEBUG (+ EXTRA RS232)

The J960 connector is a 5x2 pins double row 2.54mm.

Figure 26 J960 detail

The connector is located as shows the figure below.

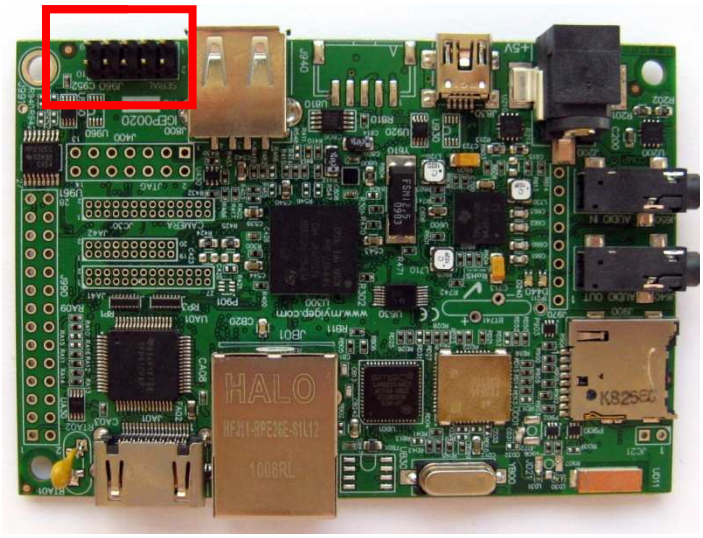


Figure 27 J960 location

On IGEPv2 revision B This J960 connector has only Debug RS232 interface (with RS232 transceiver).

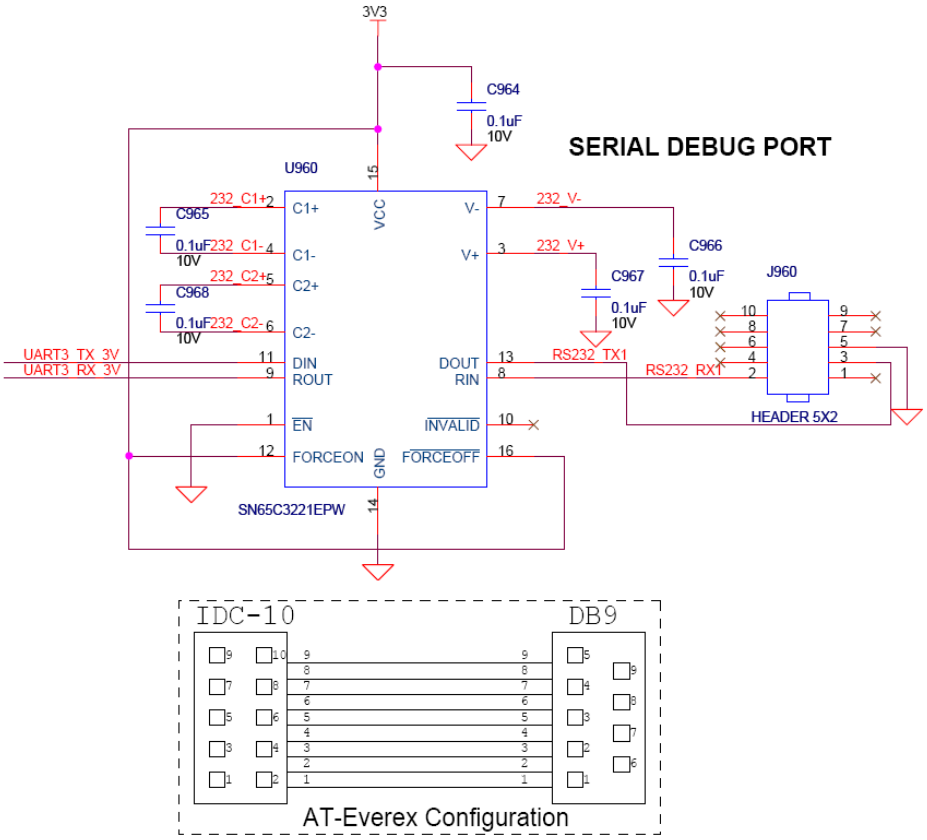


Figure 28 IGEPv2 revision B schematic J960

On IGEPv2 revision C several features have been added:

***NOTE*: Contact ISEE sales for custom assembly boards.**

- Additional RS232 port (UART1) on same J960 connector. It is only needed to rotate 180º the IDC-10 (AT-Everex) to DB9 cable.
- It has been added resistors for alternative UART1, UART2 and UART3 hardware selection.

Also, IGEPv2 revision C series have debug RS232 interface with transceiver (UART3) like IGEPv2 revision B series.

The schematic below illustrate IGEPv2 revision C pin out of the connector.

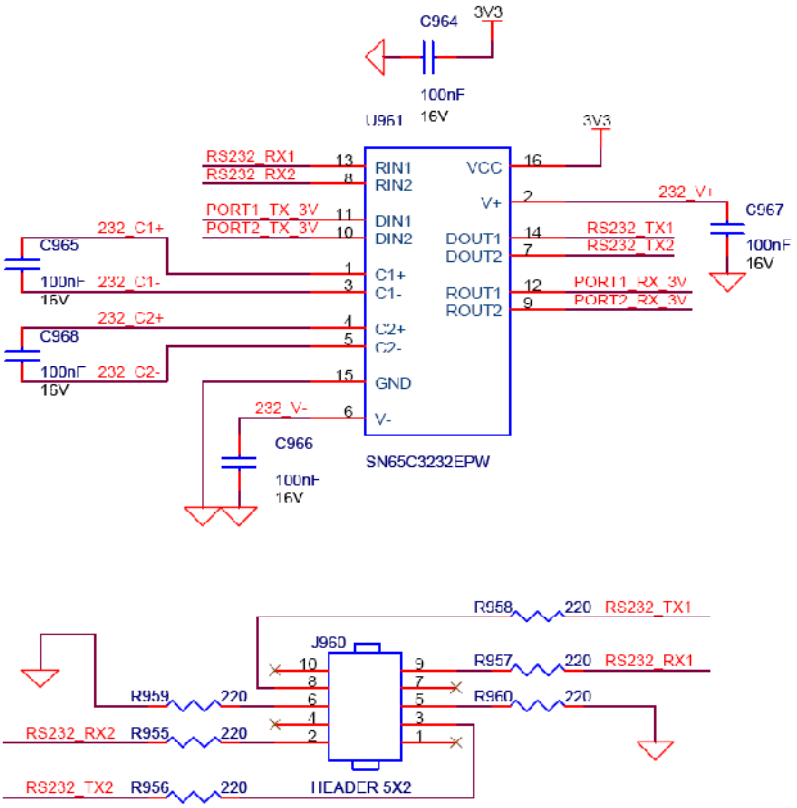


Figure 29 IGEPv2 revision C Schematic J960

First RS232 is located on J960 pins 2 and 3, and the second one on pins 8 and 9.

Next resistors enable hardware UART select to assign them on each connector.

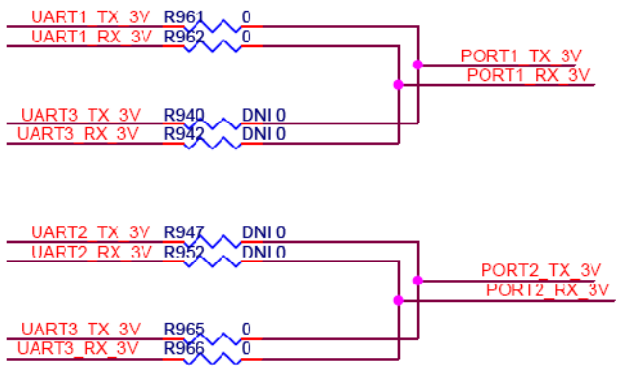


Figure 30 IGEPv2 revision C resistors for UART hardware selection

The 5x2 Header follow the IDC-10 (AT-Everex) configuration.

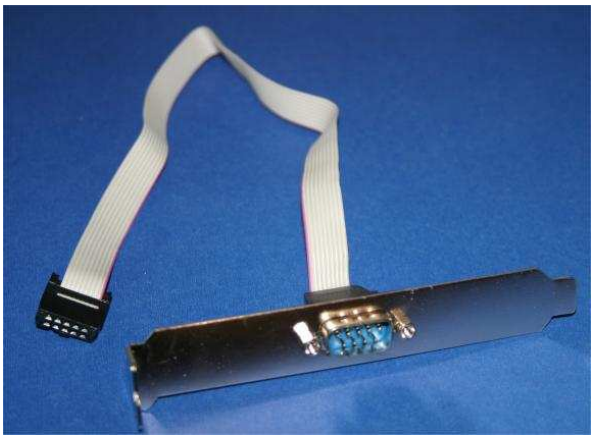


Figure 31 IDC-10 to DB9 cable

So, it is needed null modem configuration (direct connection between two computers). RX and TX lines are crossed in this null modem configuration between two equipments (TX1->RX2 / TX2->RX1).

5.5 CONNECTOR J971: KEYBOARD MATRIX 4X4

The J971 connector is an 8 pins single row 2.54mm (It is not default populated on IGEPv2 boards).

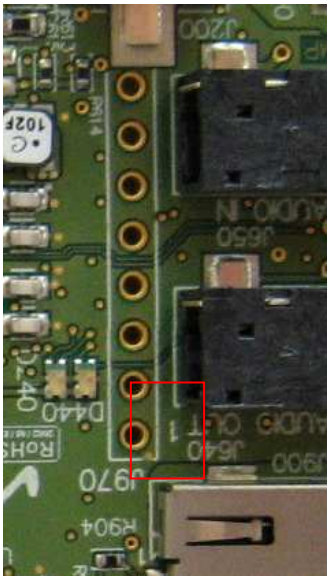


Figure 32 J971 detail

Its can be used to connect

a 4x4 keyboard matrix.

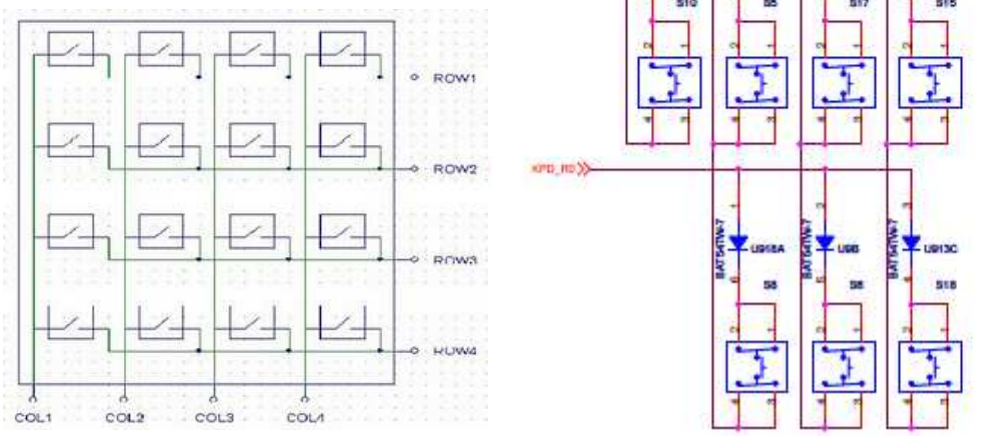


Figure 33 Keyboard matrix 4x4 and schematic example

Pin 1 is labeled on the PCB. The connector is located as shows the figure below.

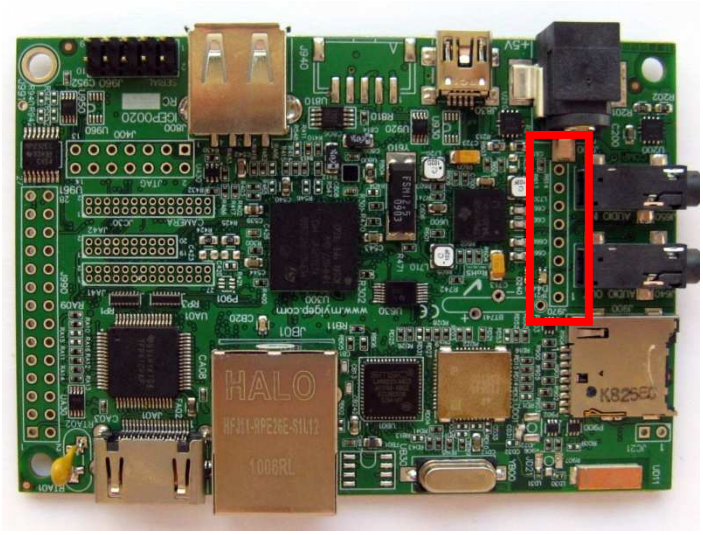


Figure 34 J971 location

The schematic below illustrate the pin out of the connector.

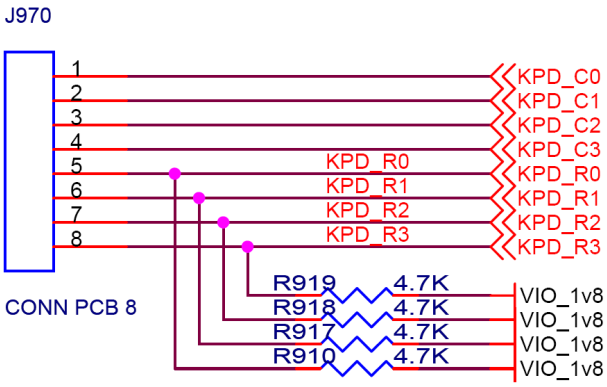


Figure 35 Schematic J971

KPD_Cx: columns

KPD_Rx: rows

When a key button of the keyboard matrix is pressed the corresponding row and column lines are shorted together. To allow key press detection, all input pins (KBR) are pulled up to VCC and all output pins (KBC) driven to a low level.

Any action on a button generates an interrupt to the sequencer.

The decoding sequence is written to allow detection of simultaneous press actions on several key buttons.

5.6 TFT CONNECTORS: JA41-JA42

There are two 1.27mm Double Row Terminal Strip for the TFT interface. Both are from SAMTEC manufacturer (Part Number FTS-110-01-L-D).

5.6.1 CONNECTOR JA41

On IGEPv2 revision B series:

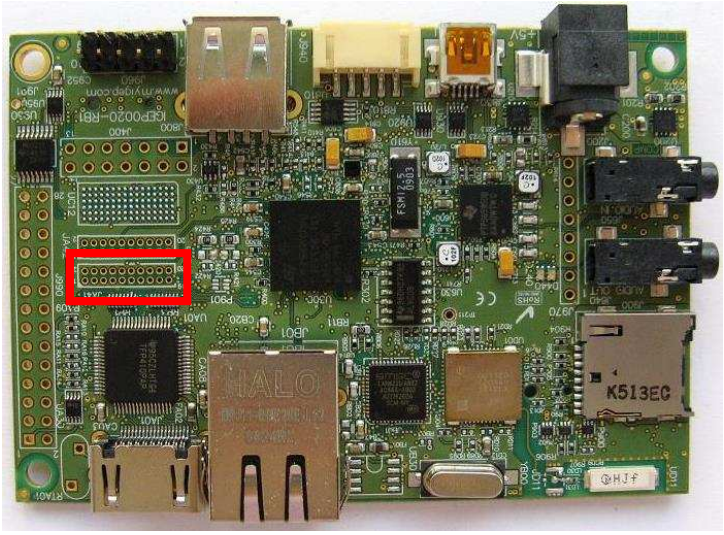


Figure 36 IGEPv2 revision B JA41 location

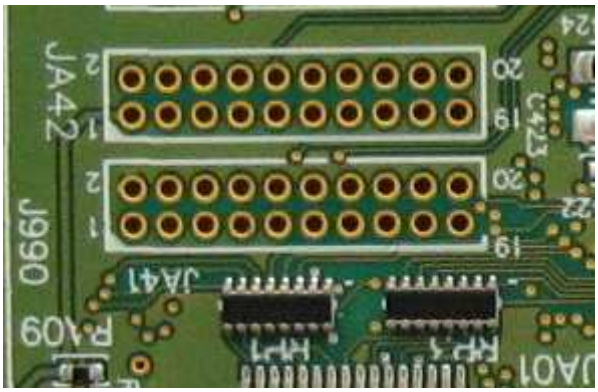


Figure 37 IGEPv2 revision B JA41-JA42 detail

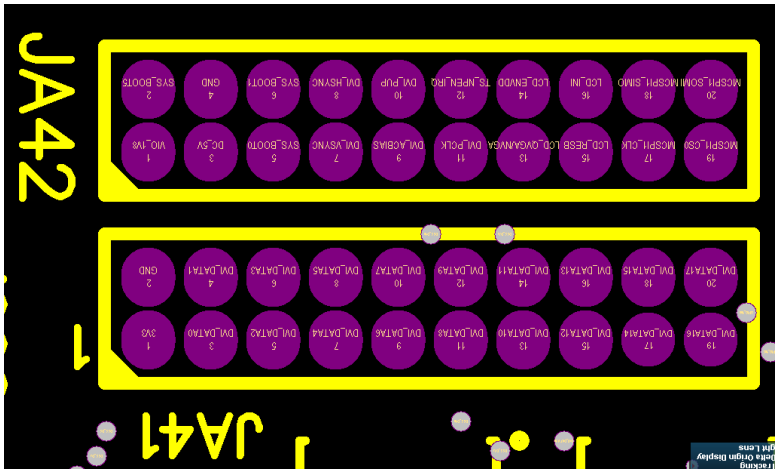


Figure 38 JA41-JA42 IGEPv2 revision B pinout detail

On IGEPv2 revision C series:

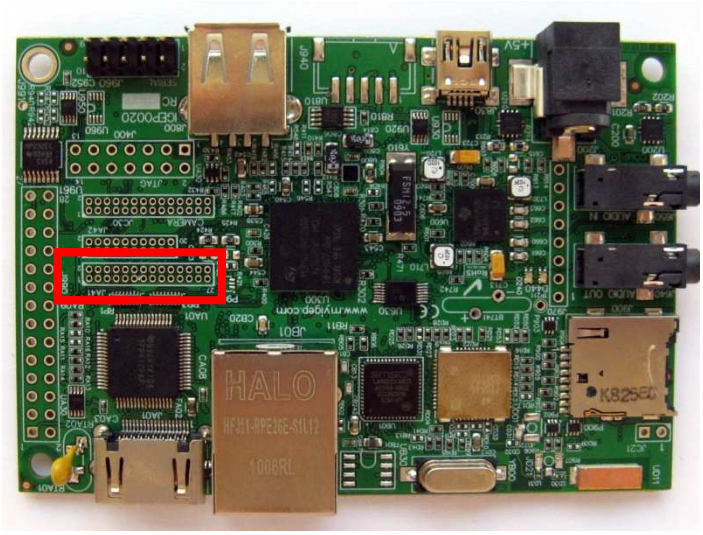


Figure 39 IGEPv2 revision C JA41 location

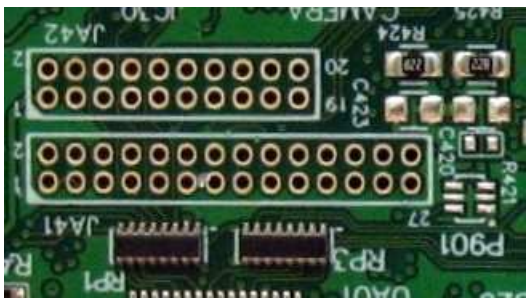


Figure 40 IGEPv2 revision C JA41 and JA42 detail

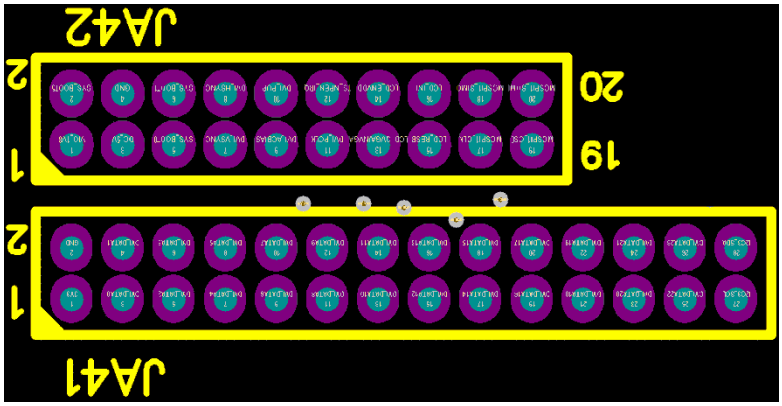


Figure 41 IGEPv2 revision C JA41-JA42 pinout detail

These connectors allow the access to the LCD signals. Next table shows the signals that are on the JA41 and JA42 connector (*shadowed cells are only available on IGEPv2 revision C series*).

Pin#	Signal	I/O	Description
1	3V3	PWR	DC rail from the Main DC supply
2	GND	PWR	Ground
3	DVI_DATA0	O	LCD Pixel Data bit
4	DVI_DATA1	O	LCD Pixel Data bit
5	DVI_DATA2	O	LCD Pixel Data bit
6	DVI_DATA3	O	LCD Pixel Data bit
7	DVI_DATA4	O	LCD Pixel Data bit
8	DVI_DATA5	O	LCD Pixel Data bit
9	DVI_DATA6	O	LCD Pixel Data bit
10	DVI_DATA7	O	LCD Pixel Data bit
11	DVI_DATA8	O	LCD Pixel Data bit
12	DVI_DATA9	O	LCD Pixel Data bit
13	DVI_DATA10	O	LCD Pixel Data bit
14	DVI_DATA11	O	LCD Pixel Data bit
15	DVI_DATA12	O	LCD Pixel Data bit
16	DVI_DATA13	O	LCD Pixel Data bit
17	DVI_DATA14	O	LCD Pixel Data bit
18	DVI_DATA15	O	LCD Pixel Data bit
19	DVI_DATA16	O	LCD Pixel Data bit
20	DVI_DATA17	O	LCD Pixel Data bit
21	DVI_DATA18	O	LCD Pixel Data bit
22	DVI_DATA19	O	LCD Pixel Data bit
23	DVI_DATA20	O	LCD Pixel Data bit
24	DVI_DATA21	O	LCD Pixel Data bit
25	DVI_DATA22	O	LCD Pixel Data bit
26	DVI_DATA23	O	LCD Pixel Data bit
27	I2C3_SCL	I/O	I2C3 interface
28	I2C3_SDA	I/O	I2C3 interface

Table 1 IGEPv2 revision B and C JA41 connector pinout

This connector can also be used for other functions on the board based on the multiplexer setting of each pin. Next table shows the options. The MUX: column

indicates which MUX mode must be set for each pin to make the respective signals accessible on the pins of the OMAP3530.

Signal	MUX:0	MUX:2	MUX:4
DVI_DATA0	DATA0	UART1_CTS	GPIO70
DVI_DATA1	DATA1	UART1_RTS	GPIO71
DVI_DATA2	DATA2	-	GPIO72
DVI_DATA3	DATA3	-	GPIO73
DVI_DATA4	DATA4	UART3_RX	GPIO74
DVI_DATA5	DATA5	UART3_TX	GPIO75
DVI_DATA6	DATA6	UART1_TX	GPIO_76
DVI_DATA7	DATA7	UART1_RX	GPIO_77
DVI_DATA8	DATA8	-	GPIO_78
DVI_DATA9	DATA9	-	GPIO_79
DVI_DATA10	DATA10	-	GPIO79
DVI_DATA11	DATA11	-	GPIO81
DVI_DATA12	DATA12	-	GPIO82
DVI_DATA13	DATA13	-	GPIO83
DVI_DATA14	DATA14	-	GPIO84
DVI_DATA15	DATA15	-	GPIO85
DVI_DATA16	DATA16	-	GPIO86
DVI_DATA17	DATA17	-	GPIO87
DVI_DATA18	DATA18	-	GPIO88
DVI_DATA19	DATA19	-	GPIO89
DVI_DATA20	DATA20	-	GPIO90
DVI_DATA21	DATA21	-	GPIO91
DVI_DATA22	DATA22	-	GPIO92
DVI_DATA23	DATA23	-	GPIO93
I2C3_SCL	I2C3_SCL	-	GPIO184
I2C3_SDA	I2C3_SDA	-	GPIO185

Table 2 IGEPv2 revision B and C JA41 connector mux

The schematic below illustrate the pin out of the connectors.

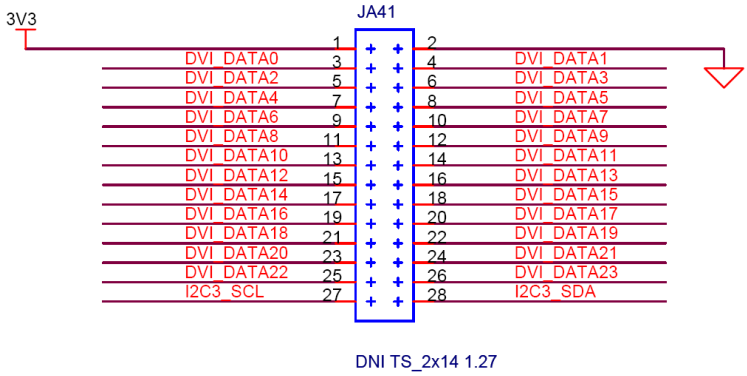


Figure 42 IGEPv2 revision C Schematic JA41

5.6.2 CONNECTOR JA42

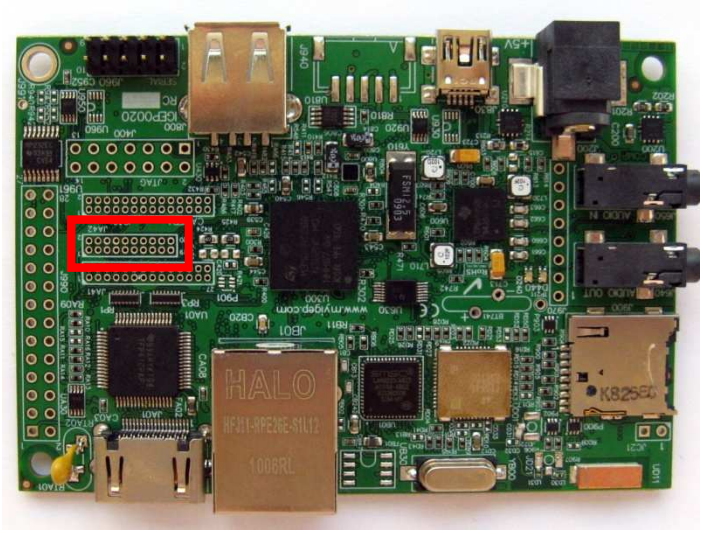


Figure 43 IGEPv2 revision B and C JA42 location

Pin#	Signal	I/O	Description
1	VIO_1V8	PWR	1.8V buffer reference rail.
2	SYS_BOOT5	I	OMAP boot config
3	DC_5V	PWR	5V reference rail.
4	GND	PWR	
5	SYS_BOOT0	I	OMAP boot config
6	SYS_BOOT1	I	OMAP boot config
7	DVI_VSYNC	O	LCD Vertical Sync
8	DVI_HSYNC	O	LCD Horizontal Sync
9	DVI_ACBIAS	O	LCD control
10	DVI_PUP	O	Control signal for the DVI controller. When Hi, DVI is enabled. Can be used to activate circuitry on adapter board if desired.
11	DVI_PCLK	O	LCD clock
12	TS_nPEN_IRQ	O	Touchscreen control
13	LCD_QVGA/nVGA	O	Touchscreen control
14	TS_ENVVDD	O	Touchscreen control
15	LCD_RESB	O	Touchscreen control
16	LCD_INI	O	Touchscreen control
17	MCSPI1_CLK	O	Touchscreen control
18	MCSPI1_SIMO	I	Touchscreen control
19	MCSPI1_CS0	O	Touchscreen control
20	MCSPI1_SOMI	O	Touchscreen control

Table 3 JA42 connector pinout

The current available on the DC_5V rail is limited to the available current that remains from the DC supply that is connected to the DC power jack on the board. Keep in mind that some of that power is needed by the USB Host power rail and if more power is needed for the expansion board, the main DC power supply current capability may need to be increased. All signals are 1.8V except the DVI_PUP which is a 3.3V signal.

The 1.8V rail is for level translation only and should not be used to power circuitry on the board. The 3.3V rail also has limited capacity on the power as well.

It is suggested that the 5V rail be used to generate the required voltages for an adapter card.

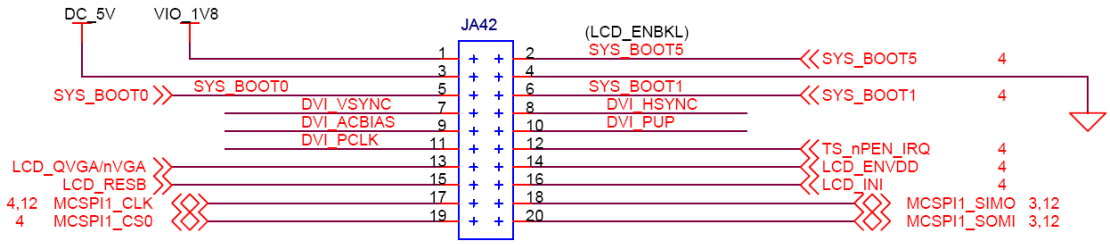


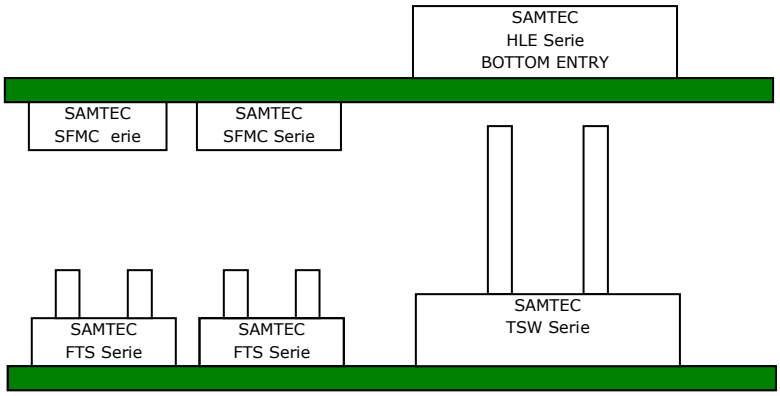
Figure 44 IGEPv2 revision B and C Schematic JA42

NOTE: JA41 and JA42 connectors are NOT BeagleBoard compatible.

WARNING: The TFT signals goes directly to OMAP processor. Improper use of this connector could result in damage of the processor.

5.6.3 CONNECTOR JA41-JA42 COUNTERPART

JA41 and JA42 mates with SFMC SAMTEC Series.



5.7 CONNECTOR J990: GPIO

The J990 connector is a 28 pins 2x14 dual row 2.54mm.

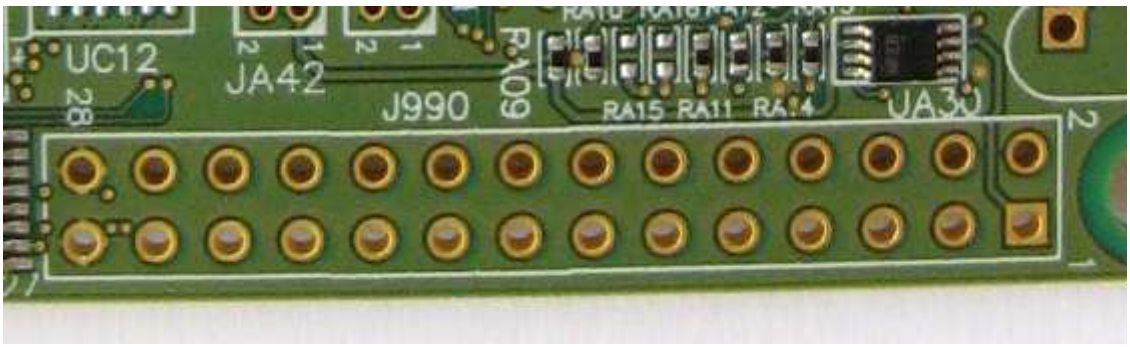


Figure 45 J990 detail

Pins 1, 2, 27 and 28 are labeled on PCB.

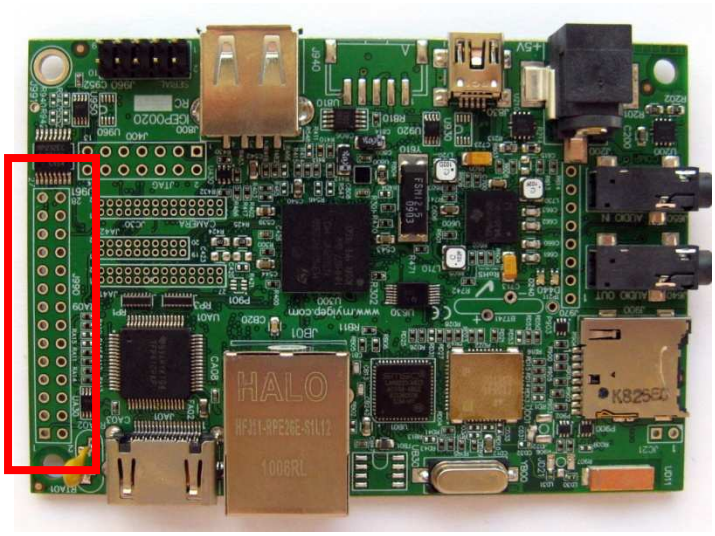


Figure 46 J990 location

The schematic below illustrate the pin out of the connectors.

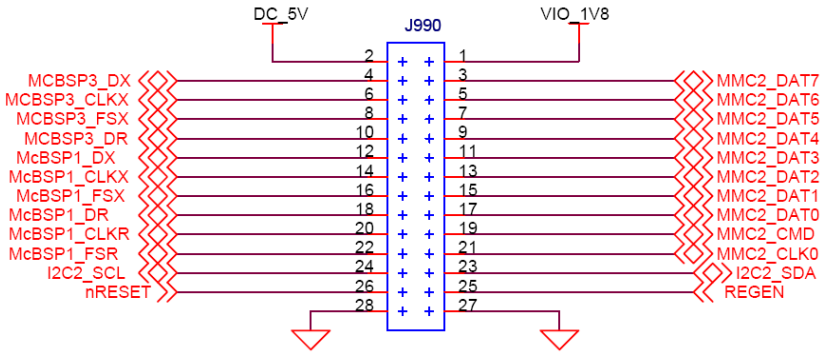


Figure 47 Schematic J990

Pin 1, 2, 27 and 28 are labeled on the PCB.

Using this expansion connector you have access to McBSP1, McBSP3, I2C2, MMC2 (8 bits), nReset and REGEN signals from OMAP Processor. The interface is at 1.8V on all signals. Only 1.8V CMOS levels are supported. **DO NOT expose the header to 3.3V.**

J990 connector is BeagleBoard compatible(*) expansion connector (http://beagleboard.org).

(*) IGEPv2-NOWIFI board is fully compatible. Other IGEPv2 board versions need software configuration to disable wifi interface and others because of shared hardware lines.

MMC2 interface is used by wifi module.

McBSP3 interface is used by PCM TPS65950 interface.

Pin	MUX:0	MUX:1	MUX:2	MUX:4
1	VIO_1V8			
2	DC_5V			
3	MMC2_DAT7			GPIO_139
4	McBSP3_DX	UART2_CTS		GPIO_140
5	MMC2_DAT6			GPIO_138
6	McBSP3_CLKX	UART2_TX		GPIO_142
7	MMC2_DAT5			GPIO_137
8	McBSP3_FSX	UART2_RX		GPIO_143
9	MMC2_DAT4			GPIO_136
10	McBSP3_DR	UART2_RTS		GPIO_141
11	MMC2_DAT3	McSPI3_CS0		GPIO_135
12	McBSP1_DX	McSPI4_SIMO	McBSP3_DX	GPIO_158
13	MMC2_DAT2	McSPI3_CS1		GPIO_134
14	McBSP1_CLKX		McBSP3_CLKX	GPIO_162
15	MMC2_DAT1			GPIO_133
16	McBSP1_FSX	McSPI4_CS0	McBSP3_FSX	GPIO_161
17	MMC2_DAT0	McSPI3_SOMI		GPIO_132
18	McBSP1_DR	McSPI4_SOMI	McBSP3_DR	GPIO_159
19	MMC2_CMD	McSPI3_SIMO		GPIO_131
20	McBSP1_CLKR	McSPI4_CLK		GPIO_156
21	MMC2_CLKO	McSPI3_CLK		GPIO_130
22	McBSP1_FSR			GPIO_157
23	I2C2_SDA	GPIO_183		
24	I2C2_SCL	GPIO_168		
25	REGEN			
26	nRESET			
27	GND			

28	GND

Table 4 Expansion Connector signals

If you use these signals in their respective groups and that is the only function you use, all of the signals are available. Whether or not the signals you need are all available, depends on the muxing function on a per-pin basis. Only one signal per pin is available at any one time.

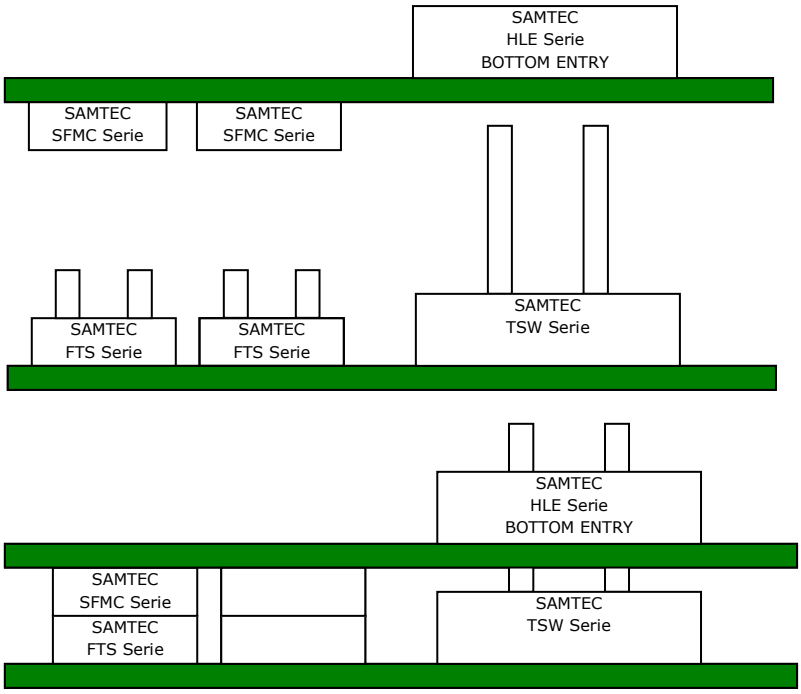
Signal	Description	I/O	Pin
SD/MMC Port 2			
MMC2_DAT7	SD/MMC data pin 7.	I/O	3
MMC2_DAT6	SD/MMC data pin 6.	I/O	5
MMC2_DAT5	SD/MMC data pin 5.	I/O	7
MMC2_DAT4	SD/MMC data pin 4.	I/O	9
MMC2_DAT3	SD/MMC data pin 3.	I/O	11
MMC2_DAT2	SD/MMC data pin 2.	I/O	13
MMC2_DAT1	SD/MMC data pin 1.	I/O	15
MMC2_DAT0	SD/MMC data pin 0.	I/O	17
MMC2_CMD	SD/MMC command signal.	I/O	19
MMC_CLKO	SD/MMC clock signal.	O	21
McBSP Port 1			
McBSP1_DR	Multi channel buffered serial port receive	I	18
McBSP1_CLKS	----------	N/A	N/A
McBSP1_FSR	Multi channel buffered serial port transmit frame sync RCV	I/O	22
McBSP1_DX	Multi channel buffered serial port transmit	I/O	12
McBSP1_CLKX	Multi channel buffered serial port transmit clock	I/O	14
McBSP1_FSX	Multi channel buffered serial port transmit frame sync XMT	I/O	16
McBSP1_CLKR	Multi channel buffered serial port receive clock	I/O	20
I2C Port 2			
I2C2_SDA	I2C data line.	IOD	23
I2C2_SCL	I2C clock line	IOD	24
McBSP Port 3			
McBSP3_DR	Multi channel buffered serial port receive	I	10,18
McBSP3_DX	Multi channel buffered serial port transmit	I/O	4,12
McBSP3_CLKX	Multi channel buffered serial port receive clock	I/O	6,14
McBSP3_FSX	Multi channel buffered serial port frame sync transmit	I/O	8,16
General Purpose I/O Pins			
GPIO_130	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	21
GPIO_131	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	19
GPIO_132	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	17
GPIO_133	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	15
GPIO_134	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	13
GPIO_135	General Purpose Input/Output pin. Can be	I/O	11

	used as an interrupt pin.		
GPIO_136	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	9
GPIO_137	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	7
GPIO_138	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	5
GPIO_139	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	3
GPIO_140	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	4
GPIO_141	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	10
GPIO_142	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	6
GPIO_143	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	8
GPIO_156	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	20
GPIO_158	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	12
GPIO_159	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	18
GPIO_161	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	16
GPIO_162	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	14
GPIO_168	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	24
GPIO_183	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	23
GPIO_144	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	4
GPIO_146	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	6
GPIO_145	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	10
McSPI Port 3			
McSPI3_CS0	Multi channel SPI chip select 0	O	11
McSPI3_CS1	Multi channel SPI chip select 1	O	13
McSPI3_SIMO	Multi channel SPI slave in master out	I/O	19
McSPI3_SOMI	Multi channel SPI slave out master in	I/O	17
McSPI3_CLK	Multi channel SPI clock	I/O	21
McSPI Port 4			
McSPI4_SIMO	Multi channel SPI slave in master out	I/O	12
McSPI4_SOMI	Multi channel SPI slave out master in	I/)	18
McSPI4_CS0	Multi channel SPI chip select 0	O	16
UART Port 2			
UART2_CTS	UART clear to send	I/O	4
UART2_RTS	UART request to send	O	10
UART2_RX	UART receive	I	8
UART2_TX	UART transmit	O	6
GPT_PWM			
GPT9_PWMEVT	PWM or event for GP timer	O	4
GPT11_PWMEVT	PWM or event for GP timer	O	10
GPT10_PWMEVT	PWM or event for GP timer	O	8

Table 5 Expansion Connector signals

WARNING: The GPIO signals go directly to OMAP processor. Improper use of this connector could result in damage of the processor.

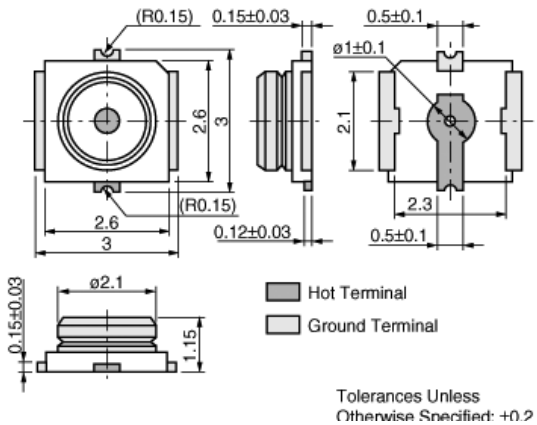
J990 mates with SAMTEC HLE series for bottom entry connection:



5.8 IGEPv2 ANTENNAS (INTERNAL/EXTERNAL - UD11, JD21, JD22)

On IGEPv2 revision B series:

JD11 is a GSC connector for the external WIFI interface. It is a MURATA GSC connector, Part number MM9329-2700RA1.



ecification

JD11 detail

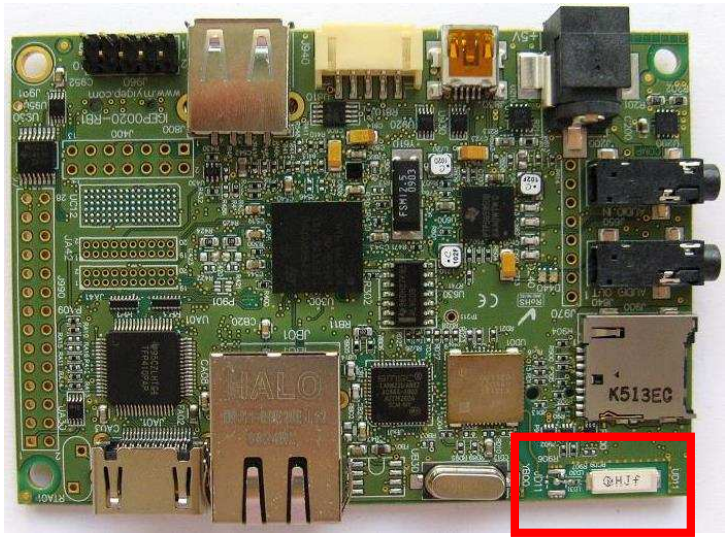


Figure 50 IGEPv2 revision B JD11 location

For the cable you will find cable assemblies if you look for CABLE ASSEMBLY RF GSM MURATA to SMA MALE.

On IGEPv2 revision C series:

JD21 and JD22 are U.FL series HIROSE connector for the external WIFI/BLUETOOTH antenna (Part number U.FL-R-SMT-1).

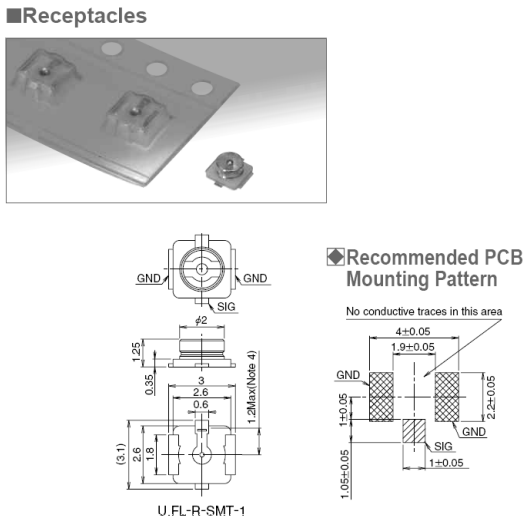


Figure 51 U.FL series receptacle connector specification

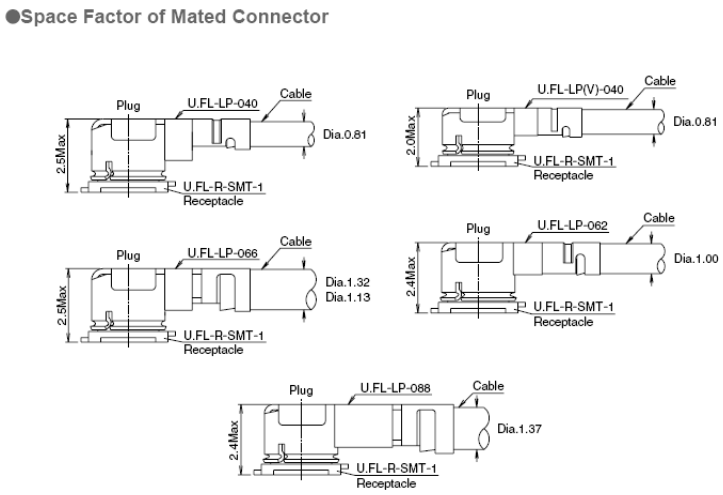


Figure 52 U.FL serie Mated connector

There are several ways to configure wifi/bluetooth antennas for IGEPv2 revision C board series.

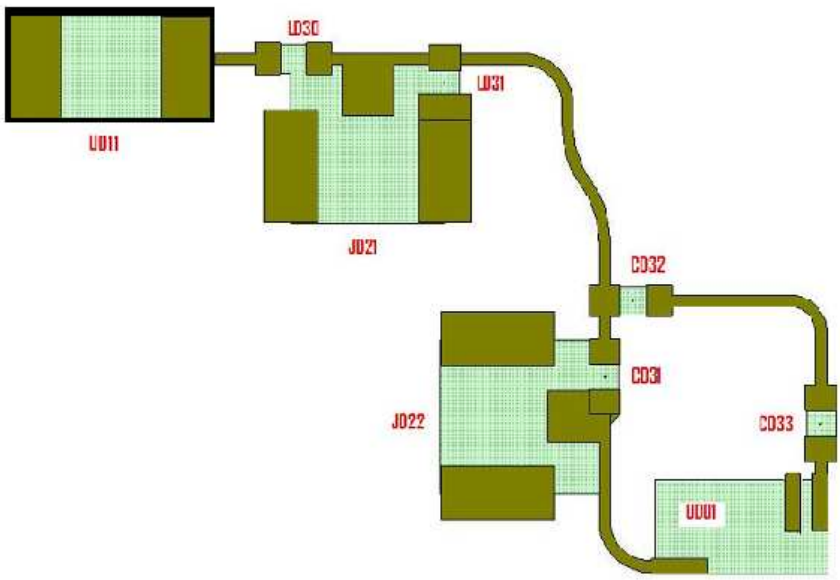


Figure 53 IGEPv2 revision C antenna layout

OPTION 1: An internal shared antenna for both BT and WIFI interfaces

This is default factory configuration for IGEPv2 revision C

UD11, LD30=1.8nH, LD31=1.5nH, CD31=15pF are populated.

JD21, JD22, CD32 and CD33 are not populated.

OPTION 2: An external shared antenna for both BT and WIFI interfaces

JD22 is populated.

JD21, UD11, LD30, LD31, CD31, CD32, and CD33 are not populated.

OPTION 3: Two external antennas for each BT and WIFI interfaces

This configuration is not available yet on wifi combo module

JD21, JD22, CD32 and CD33 are populated.

UD11, LD30, LD31, CD31 are not populated

OPTION 4: A external antenna for WIFI interface and an internal antenna for BT

This configuration is not available yet on wifi combo module

UD11, LD30, LD31, JD22, CD32 and CD33 are populated.

JD21 and CD31 are not populated

***NOTE*: Contact ISEE sales for custom assembly boards.**

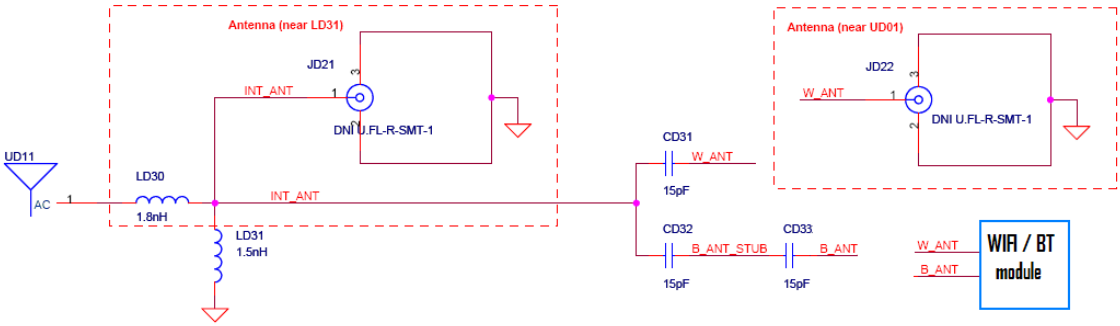


Figure 54 IGEPv2 revision C antenna schematic

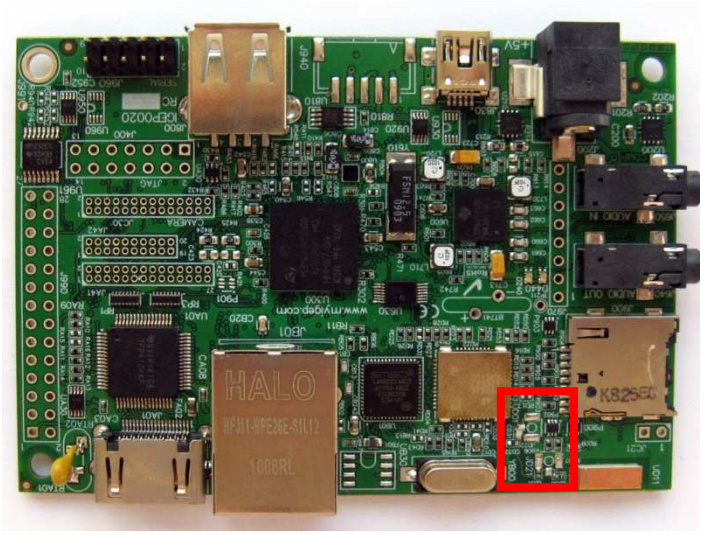


Figure 55 IGEPv2 revision C JD21, JD22 location

JD22 on yellow box (up)

JD21 on blue box (down)

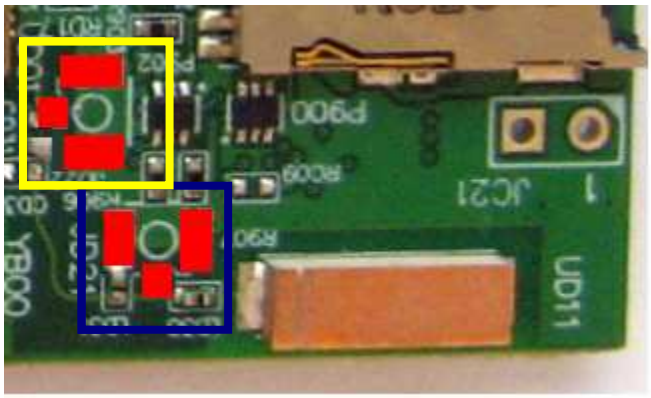


Figure 56 IGEPv2 revision C JD21, JD22 detail

5.9 CONNECTOR JC20/JC21: ANALOG TO DIGITAL CONVERTER

JC20 is a U.FL serie HIROSE connector for the analog to digital converter input (Part number U.FL-R-SMT-1).

On IGEPv2 Revision C, analog to digital converter are not default populated. [***Contact ISEE sales*** *for custom assembly boards for this feature*].

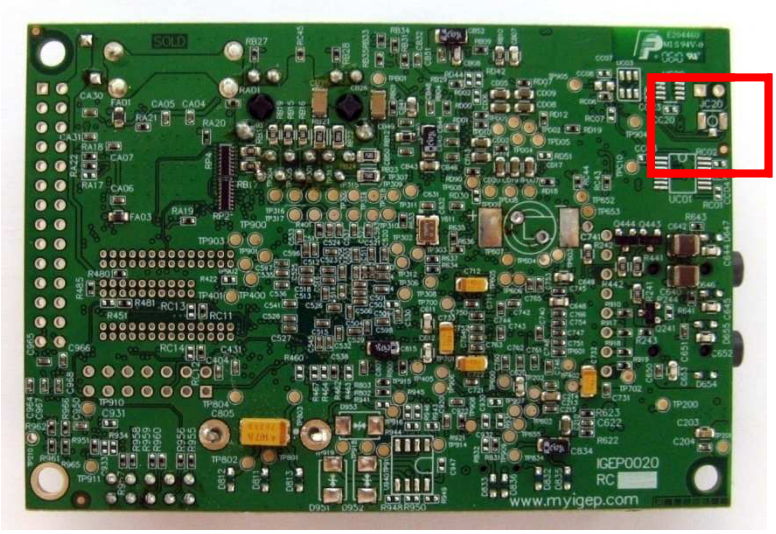


Figure 57 IGEPv2 revision C JC20 location

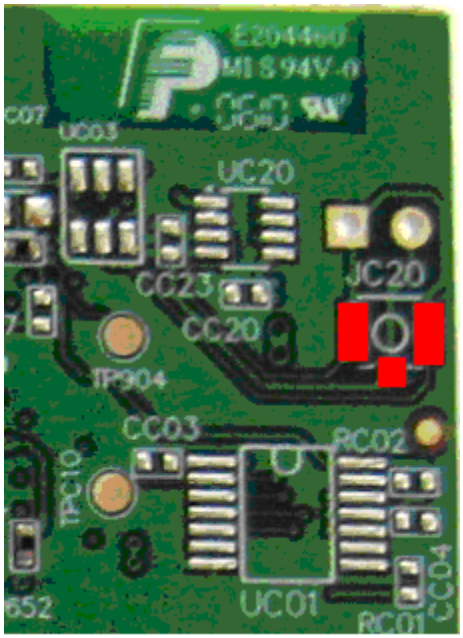


Figure 58 IGEPv2 revision C JC20 detail

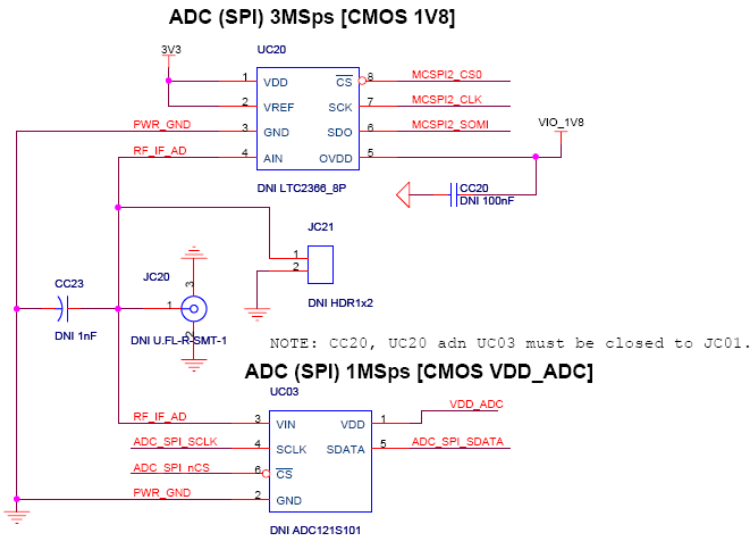


Figure 59 IGEPv2 revision C schematic A/D

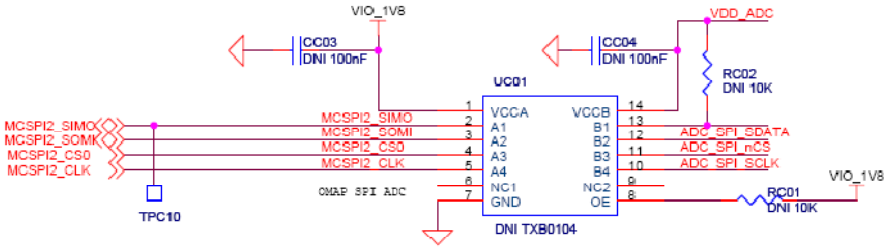


Figure 60 IGEPv2 revision C schematic A/D SPI interface

5.10 CONNECTOR JC30: CAMERA CONNECTOR

There is one 1.27mm Double Row Terminal Strip for the Camera interface from from SAMTEC manufacturer (Part Number FTS-114-01-L-D).

This JC30 connector is only available on IGEPv2 revision C series.

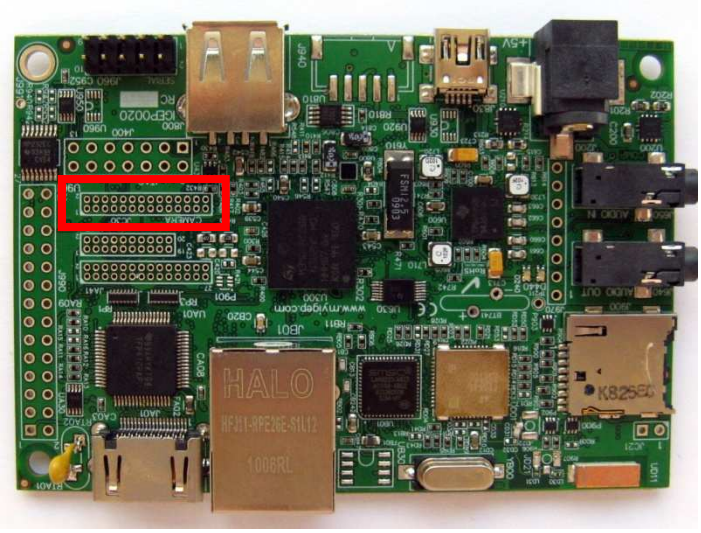


Figure 61 IGEPv2 revision C JC30 location

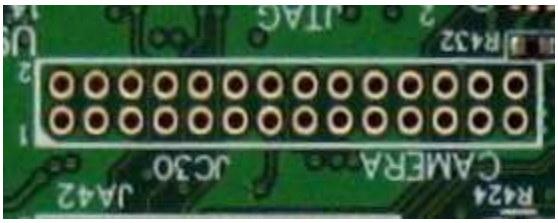


Figure 62 IGEPv2 revision C JC30 detail

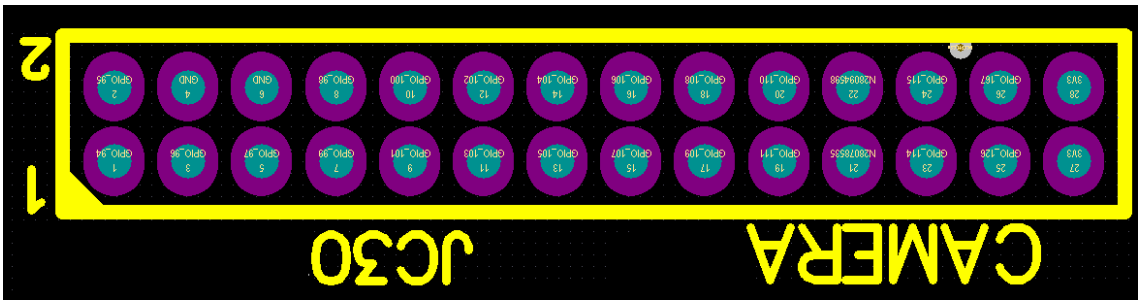


Figure 63 IGEPv2 revision C JC30 pinout detail

These connectors allow the access to the Camera interface signals. Next table shows the signals that are on the JC30 connector.

Pin#	Signal	I/O	Description
1	CAM_HS	I	Camera interface

2	CAM_VS	I	Camera interface
3	CAM_XCLKA	I	Camera interface
4	GND	PWR	
5	CAM_PCLK	I	Camera interface
6	GND	PWR	
7	CAM_D0	I	Camera interface
8	CAM_FLD	I	Camera interface
9	CAM_D2	I	Camera interface
10	CAM_D1	I	Camera interface
11	CAM_D4	I	Camera interface
12	CAM_D3	I	Camera interface
13	CAM_D6	I	Camera interface
14	CAM_D5	I	Camera interface
15	CAM_D8	I	Camera interface
16	CAM_D7	I	Camera interface
17	CAM_D10	I	Camera interface
18	CAM_D9	I	Camera interface
19	CAM_XCLKB	I	Camera interface
20	CAM_D11		Camera interface
21	GPIO_112 / I2C2_SCL		I2C interface
22	GPIO_113 / I2C2_SDA		I2C interface
23	OMAP_GPIO_114		Input
24	OMAP_GPIO_115		Input
25	CAM_STROBE		Camera interface
26	CAM_WEN		Camera interface
27	3V3	PWR	
28	3V3	PWR	

Table 6 IGEPv2 revision C JC30 connector pinout

This connector can also be used for other functions on the board based on the multiplexer setting of each pin. Next table shows the options. The MUX: column indicates which MUX mode must be set for each pin to make the respective signals accessible on the pins of the OMAP3530.

Signal	MUX:0	MUX:2	MUX:4
CAM_D0	DATA0	-	GPIO99
CAM_D1	DATA1	-	GPIO100
CAM_D2	DATA2	-	GPIO101
CAM_D3	DATA3	-	GPIO102
CAM_D4	DATA4	-	GPIO103
CAM_D5	DATA5	-	GPIO104
CAM_D6	DATA6	-	GPIO105
CAM_D7	DATA7	-	GPIO106
CAM_D8	DATA8	-	GPIO107
CAM_D9	DATA9	-	GPIO108
CAM_D10	DATA10	-	GPIO109
CAM_D11	DATA11	-	GPIO110
CAM_HS	CAM_HS	-	GPIO94
CAM_VS	CAM_VS	-	GPIO95
CAM_XCLKA	CAM_XCLKA	-	GPIO96
CAM_XCLKB	CAM_XCLKB	-	GPIO111

CAM_PCLK	CAM_PCLK	-	GPIO97
CAM_FLD	CAM_FLD	-	GPIO98
CAM_WEN	CAM_WEN	-	GPIO167
CAM_STROBE	CAM_STROBE	-	GPIO126

Table 7 IGEPv2 revision C JC30 connector mux

All signals are 1.8V.

It is suggested that the 3V3 rail be used to generate the required voltages for an adapter card.

The schematic below illustrate the pin out of the connectors.

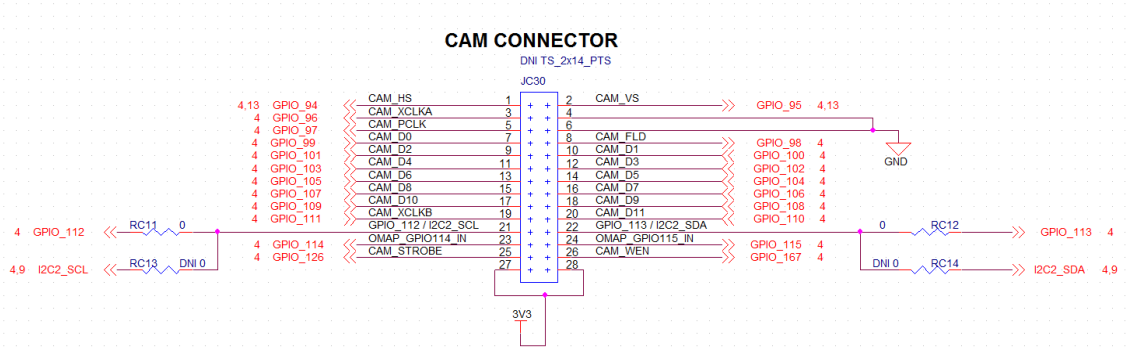


Figure 64 IGEPv2 revision C JC30 schematic

WARNING: The CAMERA signals go directly to OMAP processor. Improper use of this connector could result in damage of the processor.

5.11S_VIDEO SIGNALS (TP400 and TP401)

S-video signals are available on TP400 and TP401 test points.

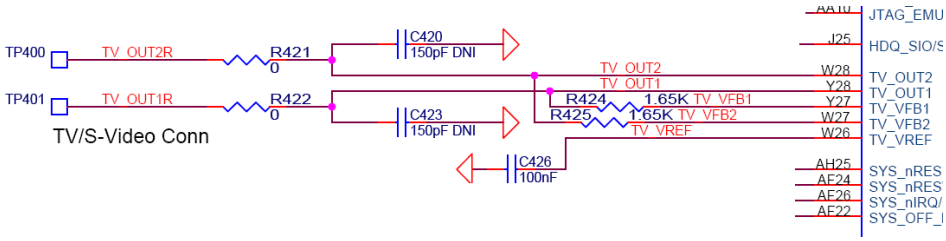


Figure 65 TP400 and TP401 schematic

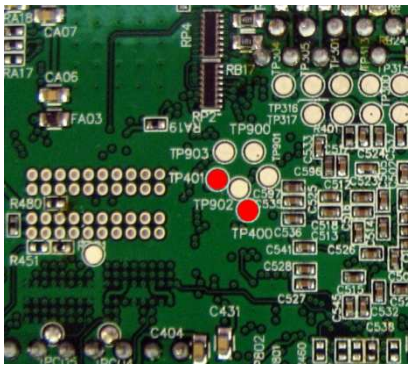


Figure 66 TP400 and TP401 location

WARNING: The VIDEO signals go directly to OMAP processor. Improper use of this connector could result in damage of the processor.

5.12 RTC BACKUP BATTERY

The TPS65950 implements a backup mode, in which the backup battery keeps the RTC running. A rechargeable backup battery can be recharged from the main battery.

This RTC feature is only available on IGEPv2 revision C series.

When the main battery is below 2.7 V or is removed, the backup battery powers the backup if the backup battery voltage is greater than 1.8 V. The backup domain powers up the following:

- Internal 32.768-kHz oscillator and RTC
- Hash table (20 registers of 8 bits each) and Eight GP storage registers

TPS65950 battery backup is available by using BT741 or C741.

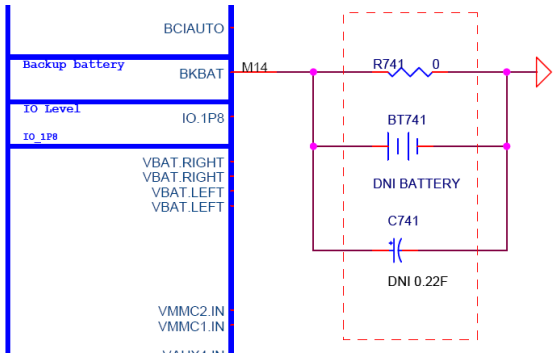
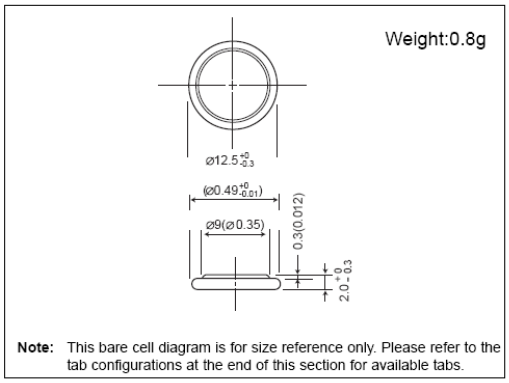


Figure 67 IGEPv2 revision C TPS65950 battery backup schematic

BT741: is Lithium Coin Battery (VL Series) from Panasonic

VL1220

■ Dimensions(mm)



Note: This bare cell diagram is for size reference only. Please refer to the tab configurations at the end of this section for available tabs.

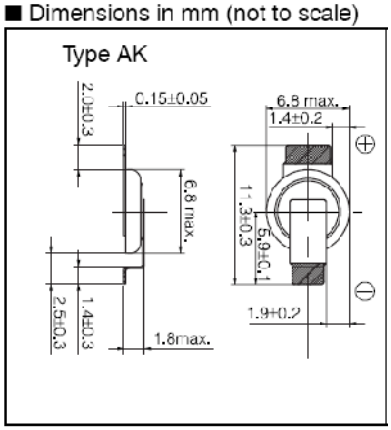
■ Specification

Nominal voltage (V)	3
Nominal capacity (mAh)	7.0
Continuous standard load (mA)	0.02
Operating temperature (C)	-20 ~ +60

Figure 68 BT741 specification

C741: is an Electric Double Layer Capacitors from PANASONIC (Serie EN)

■ Dimensions in mm (not to scale)



■ Specifications

Category temp. range	-10 to +60°C	
Maximum Operating Voltage	3.3 V .DC	
Nominal Capacitance	0.2 F	
Maximum Operating Current	10 µA MAX	
Stability at low temperature and high temperature	Category temp. range(-10°C)	
	Capacitance change	±30% of initial measured value at +20°C
	Internal resistance	≤10 times of initial measured value at +20°C
	Category temp. range(+60°C)	
	Capacitance change	±30% of initial measured value at +20°C
	Internal resistance	≤ measured value at +20°C
Endurance	After 500 hours application of 3.3V. DC at +60°C, the capacitor shall meet the following limits.	
	Capacitance change	±30% of initial measured value
	Internal resistance	4kΩ or less
Shelf Life	After 500 hours storage at +60°C without load, the capacitor shall meet the following limits	
	Capacitance change	±30% of initial measured value
	Internal resistance	1 k ohm or less
High temperature High humidity	After 500 hours storage at +40°C, 90 to 95% R.H., the capacitor shall meet the specified limits for shelf life.	

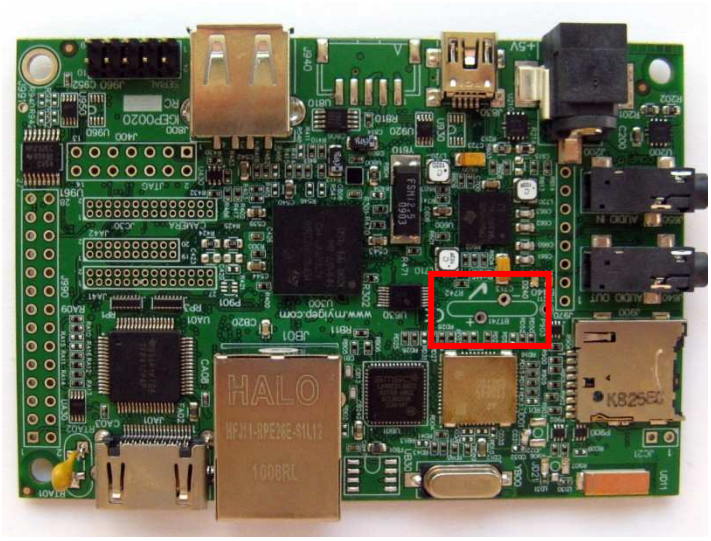


Figure 69 IGEPv2 revision C BT741 location

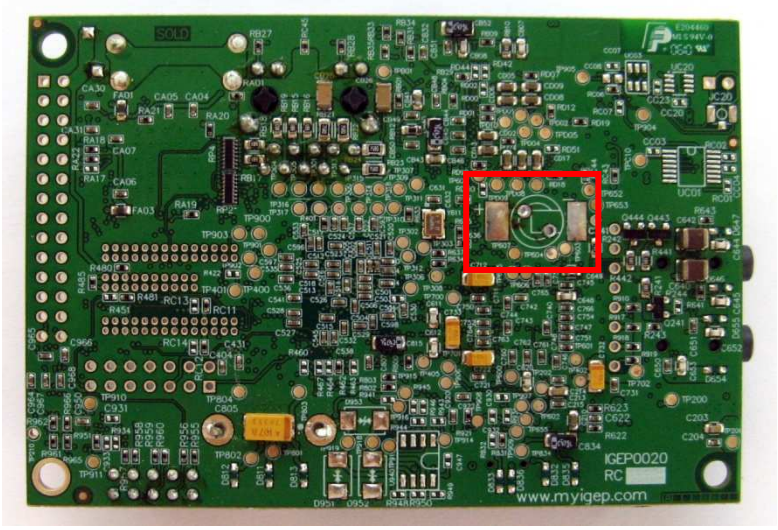


Figure 70 IGEPv2 revision C C741 location

ATTENTION: If battery is needed, resistor R741 must be unmounted.

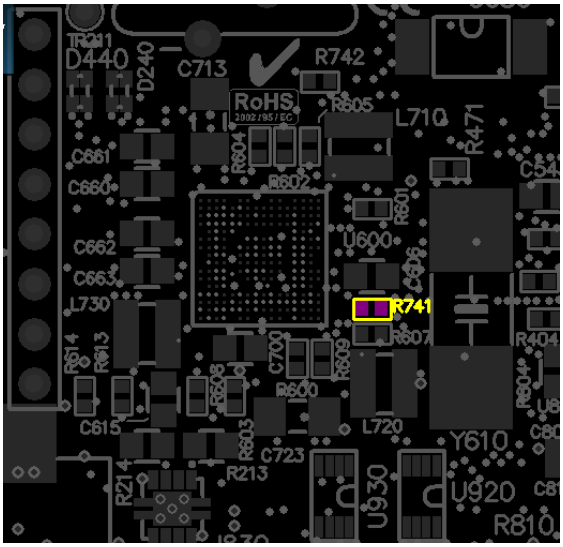


Figure 71 R741 location

6 BOARD REFERENCE

How is IGEPv2 designed?

Product Name: IGEP0020-RC1

Revision ID: RA, RB, RC, Rx (x revision family)

Revision Number: 1, 2, 3 … (n ID revision).

This manual is for Boards designed as IGEP0020-RC1

7 LIST OF FIGURES

8 CHANGELOG

Revision 1.00 (IGEP-0020-RAx):

- Initial draft

Revision 1.02 (IGEP-0020-RAx):

- Main Memory changed to 4GB/4GB 200 Mhz.

Revision 1.10 (IGEP-0020-RBx):

- This manual applies IGEP-0020-RBx boards.
- Added Wifi+Bluetooth pad for use an external antenna.
- Change LED's location and use low power high intensity leds.
- Add RS-232 transceiver for serial debug, now is compatible with serial debug that use the beagleboard.

Revision 1.11 (IGEP-0020-RBx):

- Mux table on J990 GPIO (Chapter 5.7 CONNECTOR J990: GPIO)
- Mux table on JA41-42 : TFT

Revision 1.12 (IGEP-0020-RBx):

- Corrections on mux table on J990 GPIO (Chapter 5.7 CONNECTOR J990: GPIO)

Revision 1.13 (IGEP-0020-RBx):

- Note: it is not possible to power the board with the OTG connector.
- Add new chapter: S_VIDEO SIGNALS
- Add new chapter: BATTERY BACKUP
- IGEPv2 board warranty 1 year

Revision 1.14 (IGEP-0020-RBx):

- Add comments about null modem configuration

Revision 1.15 (IGEP-0020-RCx):

- Update Hardware Manual to IGEPv2 revision C (IGEP-0020-RCx)

Revision 1.16 (IGEP-0020-RCx):

- Add some comments and extra information

Revision 1.17 (IGEP-0020-RCx):

- JD21 cannot be used as Bluetooth external antenna connector
- Add new chapter: WIFI/BLUETOOTH INTERFACE

Revision 1.18 (IGEP-0020-RCx):

- Corrections on mux table on J990 GPIO (Chapter 5.7 CONNECTOR J990: GPIO)

Revision 1.19 (IGEP-0020-RCx):

- WIFI do not work at 5GHz

Revision 1.20

- External shared antenna configuration for both BT and WIFI interfaces (chapter 5.8 IGEPV2 ANTENNAS)

Revision 1.21

- CAMERA connector. GPIO114 and GPIO115 cannot be used as outputs. So GPIO114 cannot be used are CAM_RESET neither GPIO115 as CAM_PDN. For CAM_RESET and PDN user can use CAM_STROBE and CAM_WEN configured as GPIO.